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007_CPU_XDP_

008_CPU_MISC,JTAG

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020_CPU_PCH_CSI2,EMMC,CNV

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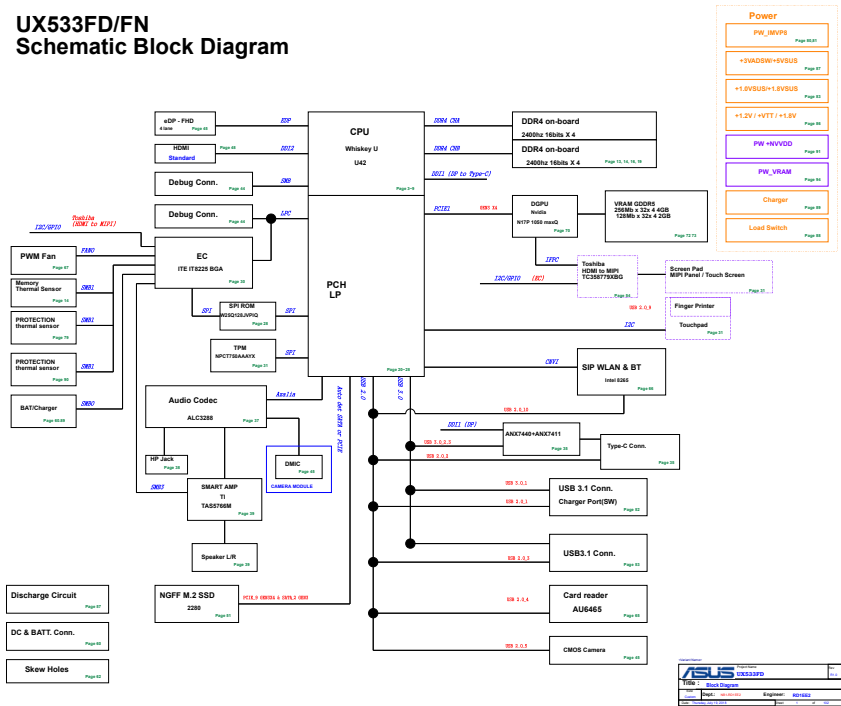
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UX533FD/FN
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UX461UN R2.1 SKU Table

MB	805 90W 9/16	CPU (On Board)	DDR (On Board)	SSD (On Board)	VRM (On Board)
	15-042 S1001-01480600	40 V08B0000-RM1000			
	17-042 S1001-01480700	80 V08B0000-RM2000			
		160 V08B0000-RM3000			
UX461UN	608B0000-MB1110	40 V08B0000-RM1000			
	15-042 S1001-01480600				
	608B0000-MB2120	80 V08B0000-RM2000			
	17-042 S1001-01480700	160 V08B0000-RM3000			
	608B0000-MB3120				
	15-042 S1001-01480600				
	608B0000-MB2121	80 V08B0000-RM2000			
	17-042 S1001-01480700	160 V08B0000-RM3000			

VRM Type : (GDDR5 2048 x 16 (For R17S-LG))

VRM Type	VRM Pin	Stop	Pinout Stop
VRM Type	VRM Pin	Stop	Pinout Stop
VRM Type	VRM Pin	Stop	Pinout Stop

DDR Type : (DDR4)

NO.	SAM_4G	MICRON_4G	SAM_8G	MICRON_8G	SAM_16G	MICRON_16G
DIMM_SEL0	L	L	H	H	H	H
DIMM_SEL1	L	H	L	H	L	H
DIMM_SEL2	L	L	L	L	H	H

1. SAMSUNG_40 03009-00400000 L903 2133 256M*32 FBGA178 QFP//SAMSUNG/K4E8E3248B-B0CG
2. SAMSUNG_40 03009-00400000 L903 2133 256M*32 FBGA178 QFP//SAMSUNG/K4E8E3248B-B0CG
3. SAMSUNG_40 03009-00400000 L903 2133 256M*32 FBGA178 QFP//SAMSUNG/K4E8E3248B-B0CG
4. SAMSUNG_40 03009-00400000 L903 2133 256M*32 FBGA178 QFP//SAMSUNG/K4E8E3248B-B0CG
5. SAMSUNG_40 03009-00400000 L903 2133 256M*32 FBGA178 QFP//SAMSUNG/K4E8E3248B-B0CG
6. SAMSUNG_40 03009-00400000 L903 2133 256M*32 FBGA178 QFP//SAMSUNG/K4E8E3248B-B0CG

UX461UN

Mount	Unmount	Mount	Unmount
N/A /GDDR5 /LCD_FUSE /WLAN_MGMT /RAM /THERMAL /VGA /VGA /VRAM_MICRON /VRAM_SAMSUNG /SPV_FP	S/PM2 /GDDR5_CODEC S /WLAN_MGMT S/PM2 /THERMAL /VGA /VGA /VRAM_MICRON /VRAM_SAMSUNG /SPV_FP	N/A /GDDR5 /LCD_FUSE /WLAN_MGMT /RAM /THERMAL /VGA /VGA /VRAM_MICRON /VRAM_SAMSUNG /SPV_FP	S/PM2 /GDDR5_CODEC S /WLAN_MGMT S/PM2 /THERMAL /VGA /VGA /VRAM_MICRON /VRAM_SAMSUNG /SPV_FP

JP	NUT (BOT)
R2P8902	H6228 H6227 H6226 H6225 H6204 H6203 H6202 H6201



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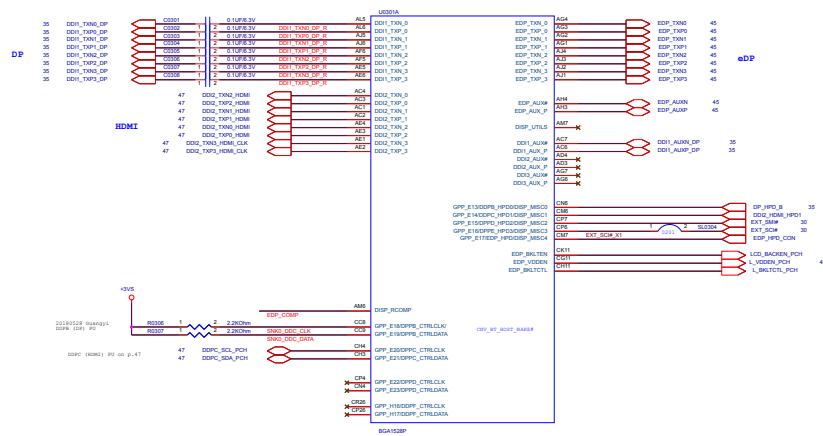


Table 5-13. DDI Disabling and Termination Guidelines

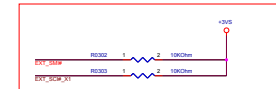
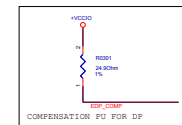
Part	Signal	How to Enable Part?	How to Disable Part?
Part 1	DDI0_CTL0DATA	PAH pin 3.3 V with 2.2 kΩ	PAH 4.75 V resistor
Part 2	DDI0_CTL0DATA	PAH pin 3.3 V with 2.2 kΩ	PAH 4.75 V resistor
Part 3	DDI0_CTL0DATA	PAH pin 3.3 V with 2.2 kΩ	PAH 4.75 V resistor
Part 4	DDI0_CTL0DATA	PAH pin 3.3 V with 2.2 kΩ	PAH 4.75 V resistor

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Intel Version	ASUS P/N
ES-0	01001-01540000
ES-2 (2C)	01001-01660000
ES-2 (4C)	01001-01660100

Display Port	
Port A (DDP)	DDP
Port B (DDI1)	DP
Port C (DDI2)	HDMI

HDMI	
DDI_0	Lane2
DDI_1	Lane1
DDI_2	Lane0
DDI_3	CLK

PD08543014 DDI1 mapping DDPB
DDI2 mapping DDPB

Project Name

ASUS	Project Name	Rev
UX533FD		01.0
Title :	CPU DISPLAY	
Dept. :	MD-ROTEC	Engineer: RD1EE2
Date: Thursday, July 10, 2015	Drawn	3 of 102

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- 008_CPU_MISC,JTAG
- 009_CPU_CFG,RSVD
- 010_CPU_POWER_CAP
- 011_
- 012_
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- 014_DDR4_ON-BOARD_A(1)
- 015_
- 016_DDR4_ON-BOARD_B(1)
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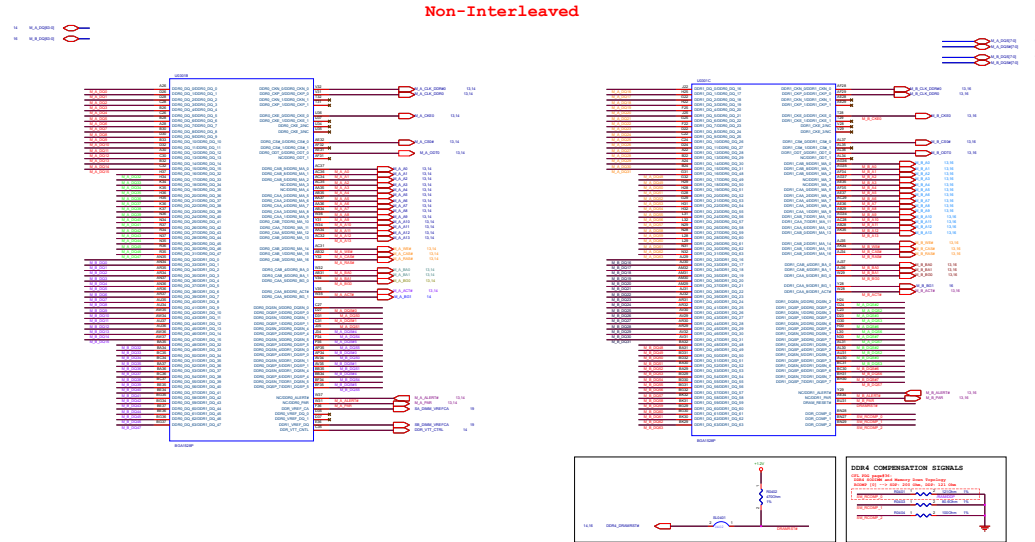
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- 019_DDR4_CA_DQ_VOLTAGE
- 020_CPU_PCH_CSI2,EMMC,CNV

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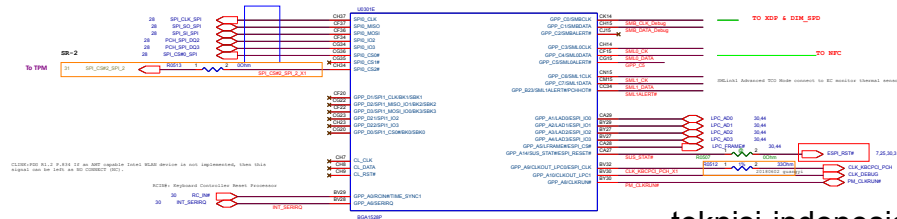
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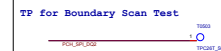
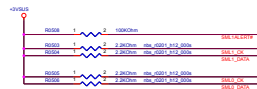
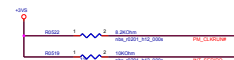
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004 CPU DDR4

005_CPU_LPC,SPI,SMB,CLINK

006_CPU_POEWR

007_CPU_XDP_

008_CPU_MISC,JTAG

009 CPU CFG,RSVD

010 CPU POWER CAP

011

012

013_DDR4_TERMINATION

014_DDR4_ON-BOARD_A(1)

015_

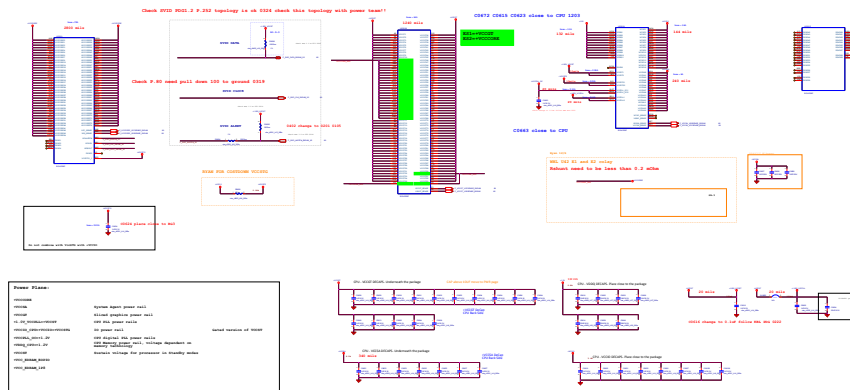
016_DDR4_ON-BOARD_B(1)

017_

018_

019_DDR4_CA_DQ_VOLTAGE

020_CPU_PCH_CSI2,EMMC,CNV



WHL Ballmap Changes

WHL ES1 will be a CFL-U43e fused down to CFL-U42

Pro Number	Pro Name	Unit	EST	Unit	EST	Unit	EST
101	PROJ. 101	Unit 1	EST 101	Unit 1	EST 101	Unit 1	EST 101
102	PROJ. 102	Unit 2	EST 102	Unit 2	EST 102	Unit 2	EST 102
103	PROJ. 103	Unit 3	EST 103	Unit 3	EST 103	Unit 3	EST 103
104	PROJ. 104	Unit 4	EST 104	Unit 4	EST 104	Unit 4	EST 104
105	PROJ. 105	Unit 5	EST 105	Unit 5	EST 105	Unit 5	EST 105
106	PROJ. 106	Unit 6	EST 106	Unit 6	EST 106	Unit 6	EST 106
107	PROJ. 107	Unit 7	EST 107	Unit 7	EST 107	Unit 7	EST 107
108	PROJ. 108	Unit 8	EST 108	Unit 8	EST 108	Unit 8	EST 108
109	PROJ. 109	Unit 9	EST 109	Unit 9	EST 109	Unit 9	EST 109
110	PROJ. 110	Unit 10	EST 110	Unit 10	EST 110	Unit 10	EST 110
111	PROJ. 111	Unit 11	EST 111	Unit 11	EST 111	Unit 11	EST 111
112	PROJ. 112	Unit 12	EST 112	Unit 12	EST 112	Unit 12	EST 112
113	PROJ. 113	Unit 13	EST 113	Unit 13	EST 113	Unit 13	EST 113
114	PROJ. 114	Unit 14	EST 114	Unit 14	EST 114	Unit 14	EST 114
115	PROJ. 115	Unit 15	EST 115	Unit 15	EST 115	Unit 15	EST 115
116	PROJ. 116	Unit 16	EST 116	Unit 16	EST 116	Unit 16	EST 116
117	PROJ. 117	Unit 17	EST 117	Unit 17	EST 117	Unit 17	EST 117
118	PROJ. 118	Unit 18	EST 118	Unit 18	EST 118	Unit 18	EST 118
119	PROJ. 119	Unit 19	EST 119	Unit 19	EST 119	Unit 19	EST 119
120	PROJ. 120	Unit 20	EST 120	Unit 20	EST 120	Unit 20	EST 120
121	PROJ. 121	Unit 21	EST 121	Unit 21	EST 121	Unit 21	EST 121
122	PROJ. 122	Unit 22	EST 122	Unit 22	EST 122	Unit 22	EST 122
123	PROJ. 123	Unit 23	EST 123	Unit 23	EST 123	Unit 23	EST 123
124	PROJ. 124	Unit 24	EST 124	Unit 24	EST 124	Unit 24	EST 124
125	PROJ. 125	Unit 25	EST 125	Unit 25	EST 125	Unit 25	EST 125
126	PROJ. 126	Unit 26	EST 126	Unit 26	EST 126	Unit 26	EST 126
127	PROJ. 127	Unit 27	EST 127	Unit 27	EST 127	Unit 27	EST 127
128	PROJ. 128	Unit 28	EST 128	Unit 28	EST 128	Unit 28	EST 128
129	PROJ. 129	Unit 29	EST 129	Unit 29	EST 129	Unit 29	EST 129
130	PROJ. 130	Unit 30	EST 130	Unit 30	EST 130	Unit 30	EST 130
131	PROJ. 131	Unit 31	EST 131	Unit 31	EST 131	Unit 31	EST 131
132	PROJ. 132	Unit 32	EST 132	Unit 32	EST 132	Unit 32	EST 132
133	PROJ. 133	Unit 33	EST 133	Unit 33	EST 133	Unit 33	EST 133
134	PROJ. 134	Unit 34	EST 134	Unit 34	EST 134	Unit 34	EST 134
135	PROJ. 135	Unit 35	EST 135	Unit 35	EST 135	Unit 35	EST 135
136	PROJ. 136	Unit 36	EST 136	Unit 36	EST 136	Unit 36	EST 136
137	PROJ. 137	Unit 37	EST 137	Unit 37	EST 137	Unit 37	EST 137
138	PROJ. 138	Unit 38	EST 138	Unit 38	EST 138	Unit 38	EST 138
139	PROJ. 139	Unit 39	EST 139	Unit 39	EST 139	Unit 39	EST 139
140	PROJ. 140	Unit 40	EST 140	Unit 40	EST 140	Unit 40	EST 140
141	PROJ. 141	Unit 41	EST 141	Unit 41	EST 141	Unit 41	EST 141
142	PROJ. 142	Unit 42	EST 142	Unit 42	EST 142	Unit 42	EST 142
143	PROJ. 143	Unit 43	EST 143	Unit 43	EST 143	Unit 43	EST 143
144	PROJ. 144	Unit 44	EST 144	Unit 44	EST 144	Unit 44	EST 144

* Pins marked RSVD must be left as NC



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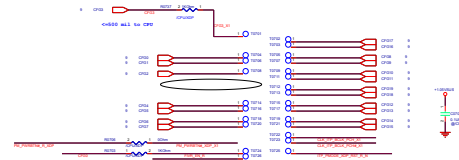
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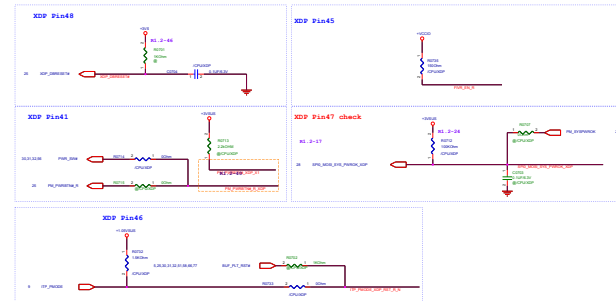
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CPU XDP connector



If need to provide system with
XDP Function, to JTAG, please
mount BCT01/BCT02

XDP will be CPU



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006_CPU_POEWR

007_CPU_XDP_

008_CPU_MISC,JTAG

009 CPU CFG,RSVD

010_CPU_POWER_CAP

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013 DDR4 TERMINATION

014_DDR4_ON-BOARD_A(1)

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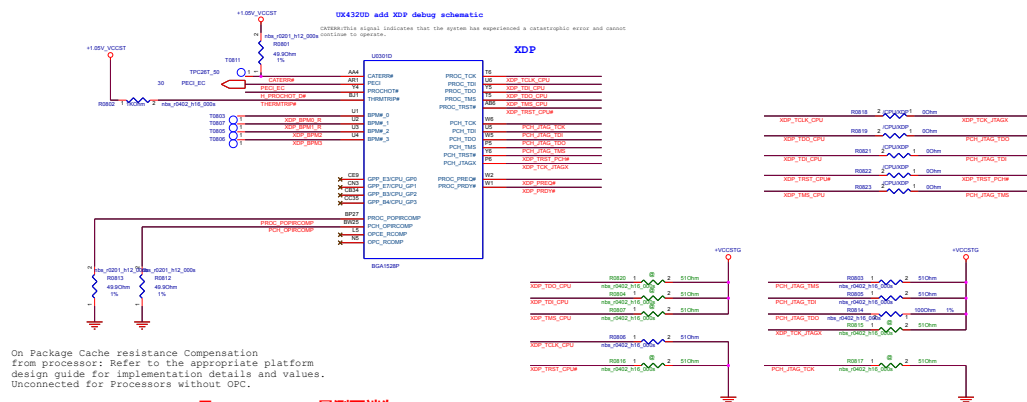
016 DDR4 ON-BOARD B(1)

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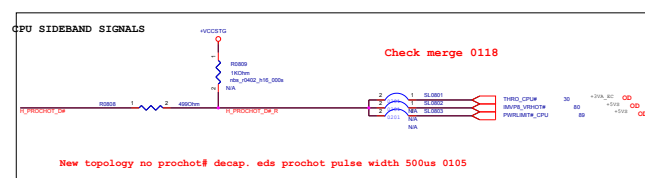
019 DDR4 CA DQ VOLTAGE

020 CPU PCH CSI2,EMMC,CNV



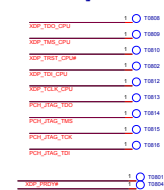
On Package Cache resistance Compensation from processor: Refer to the appropriate platform design guide for implementation details and values. Unconnected for Processors without OPC.

No OPC Check remove 且R0811 R0810量測兩端為0V 0126



```
New topology no prochot# decap. eds prochot pulse width 500us 0105
```

TP for Boundary Scan Test



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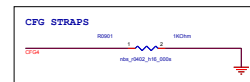
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Table 6-5. Reset and Miscellaneous Signals

Signal Name	Description	Dir.	Buffer Type	Link Type	Availability
CFG[19:0]	<p>Configuration Signals: The CFG signals have a default value of '1' if not terminated on the board. Refer to the appropriate platform design guide for pull-down recommendations when a logic low is desired.</p> <p>Intel recommends placing test points on the board for CFG pins.</p> <ul style="list-style-type: none">• CFG[0]: Stall reset sequence after PCU PLL lock until de-asserted;<ul style="list-style-type: none">1 = (Default) Normal Operation; No stall0 = Stall.• CFG[1]: Reserved configuration lane.• CFG[2]: PCI Express* Static x16 Lane Numbering Reversal.<ul style="list-style-type: none">1 = Normal operation0 = Lane numbers reversed.• CFG[3]: Reserved configuration lane.• CFG[4]: eDP enable:<ul style="list-style-type: none">1 = Disabled.0 = Enabled.• CFG[6:5]: PCI Express* Bifurcation<ul style="list-style-type: none">00 = 1 x8, 2 x4 PCI Express*01 = reserved10 = 2 x8 PCI Express*11 = 1 x16 PCI Express*• CFG[7]: PEG Training:<ul style="list-style-type: none">1 = (default) PEG Train immediately following RESET# de assertion.0 = PEG Wait for BIOS for training.• CFG[19:8]: Reserved configuration lanes.	1	GTL	SE	U - Processor Lines. CFG[2], CFG[6:5] and CFG[7] are not relevant for U - Processor Lines.

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	1	0	NOTE
CFG4	DISABLE	ENABLE	eDP ENABLE

TP for Boundary Scan Test	
TPCART_00	0: T000
TPCART_00	0: T000

ASUS	Project Name	Rev
UX533FD		01.0
Title : CPU_CFG_RSVD		
Dept:	Rev: R01E02	Engineer: R01EE2
Date: 2024.04.10.2024	Page: 9	of 100

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- 007_CPU_XDP_
- 008_CPU_MISC,JTAG
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- 016_DDR4_ON-BOARD_B(1)
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- 019_DDR4_CA_DQ_VOLTAGE
- 020_CPU_PCH_CSI2,EMMC,CNV

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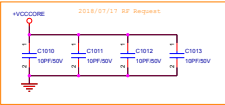
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- 002_1_SKU_Table
- 003_CPU_DISPLAY
- 004_CPU_DDR4
- 005_CPU_LPC,SPI,SMB,CLINK
- 006_CPU_POEWR
- 007_CPU_XDP_
- 008_CPU_MISC,JTAG
- 009_CPU_CFG,RSVD
- 010_CPU_POWER_CAP
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- 020_CPU_PCH_CSI2,EMMC,CNV

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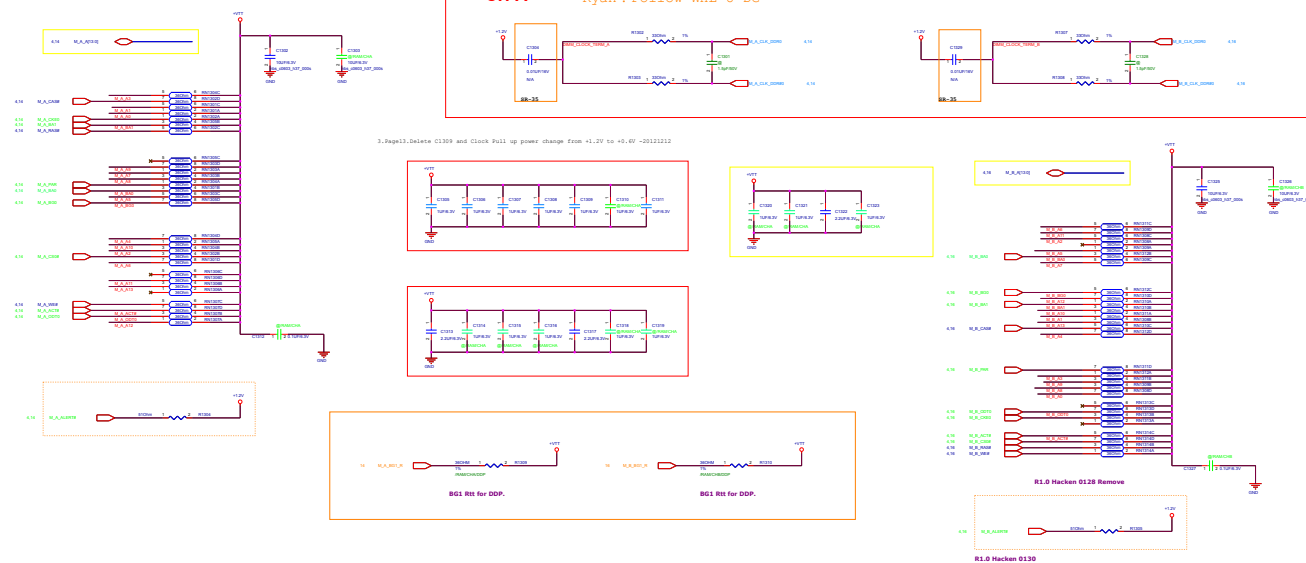
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待確認...

ASUS		Title : DDR4 TERMINATION
Part Number	Engineer	RD1022
Rev	1.0	1.0
Created	2023/03/10	2023/03/10
By	YK033FD	YK033FD

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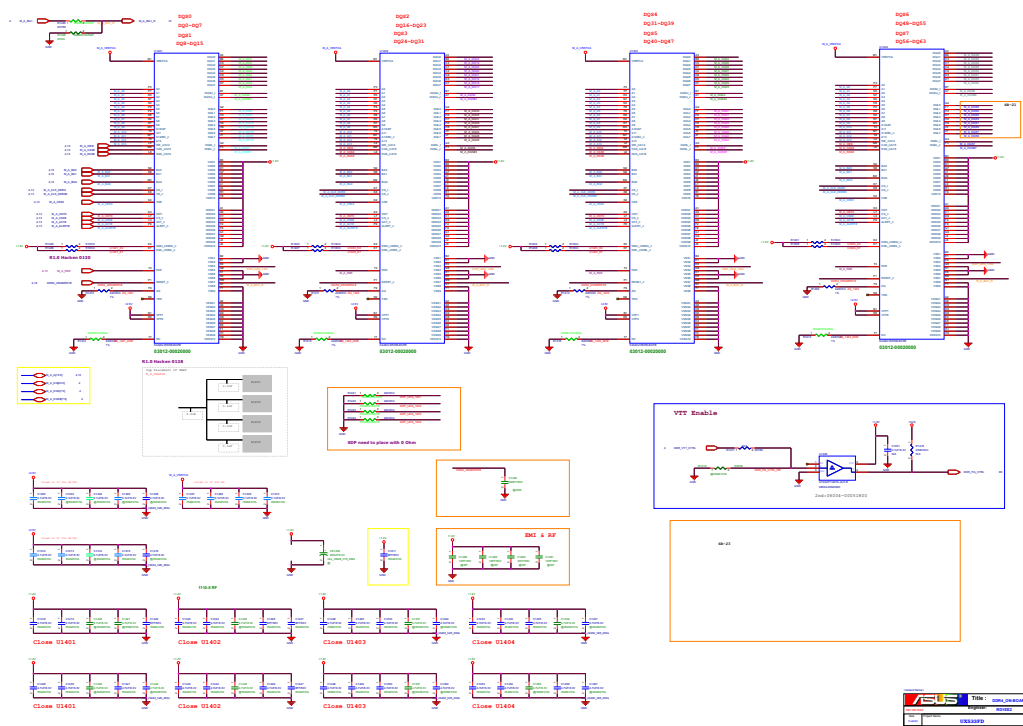
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		Title : GORLA_ONBOARD
Model : X5500-10000		Engineer : MD1082
Name :	Design :	UXS533FD

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019 DDR4 CA DQ VOLTAGE

020 CPU PCH CSI2,EMMC,CNV

021_CPU_PCH_CGPIO, LPIO, MI
SC022_CPU_PCH_AUDIO,SDIO,SD
XC

023 CPU PCH PCIE,USB,SATA

024_CPU_PCH_CLOCK SIGNAL
S,RTC

```
025 CPU PCH SYS POWER
```

026 CPU PCH POEWR,GND

027_CPU_PCH_POEWR,GND

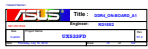
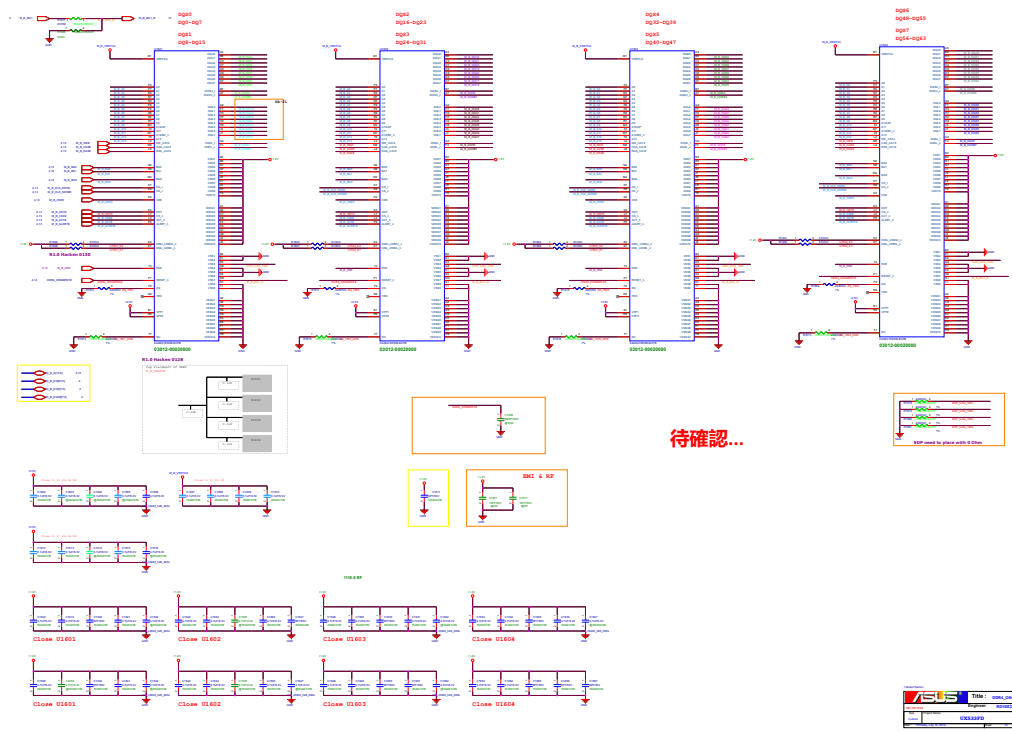
028 PCH-SPI ROM,OTH

029 ****

030 KBC IT8225

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021_CPU_PCH_CGPIO, LPIO, MI SC	
022_CPU_PCH_AUDIO,SDIO,SD XC	
023_CPU_PCH_PCIE,USB,SATA	
024_CPU_PCH_CLOCK SIGNAL S,RTC	
025_CPU_PCH_SYS_POWER	
026_CPU_PCH_POEWR,GND	
027_CPU_PCH_POEWR,GND	
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SC
022_CPU_PCH_AUDIO,SDIO,SD
XC
023_CPU_PCH_PCIE,USB,SATA
024_CPU_PCH_CLOCK SIGNAL
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025_CPU_PCH_SYS_POWER
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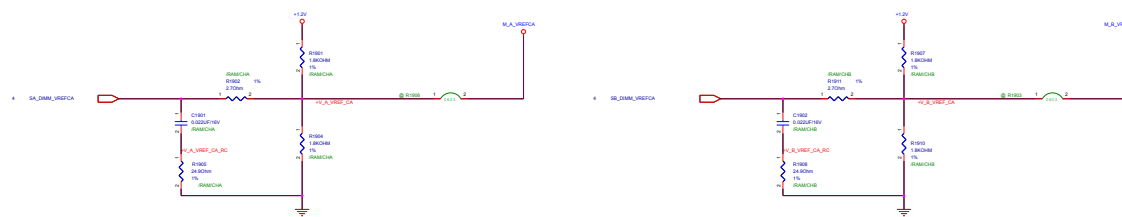
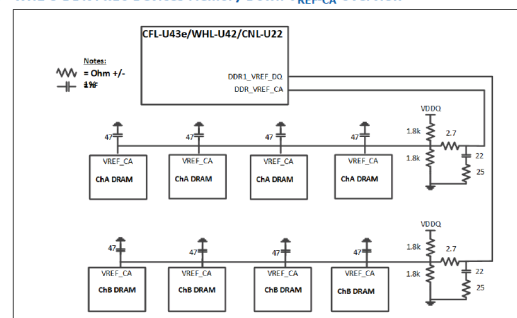


Figure 4-8. WHL U DDR4 x16 Devices Memory Down V_{REF-CA} Overview



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023_CPU_PCH_PCIE,USB,SATA
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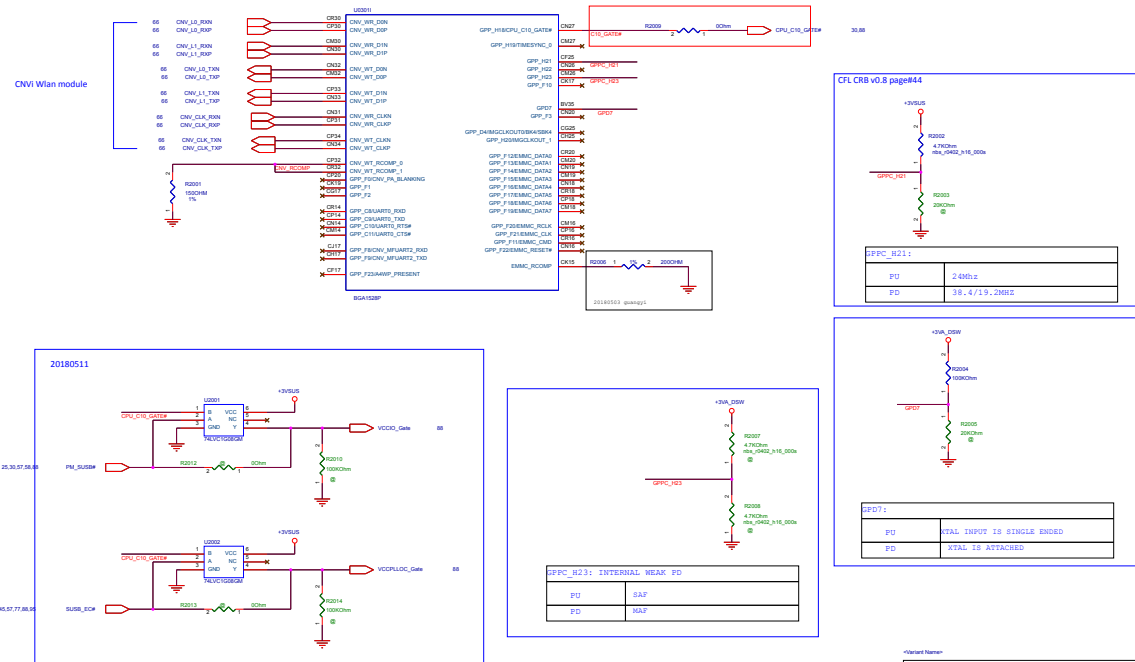
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Clipboard Manager

Project Name	Rev
ASUS UX533FD	01.0
Title : CPU PCH CSQ,EMMC	
Size	Dept. : HW-ROB22
Engineer: RD1EE2	
Date: Thursday, July 15, 2016	Page 25 of 102

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019 DDR4 CA DQ VOLTAGE

020 CPU PCH CSI2,EMMC,CNV

021_CPU_PCH_CGPIO, LPIO, MI
SC022_CPU_PCH_AUDIO,SDIO,SD
XC

023 CPU PCH PCIE,USB,SATA

024_CPU_PCH_CLOCK SIGNAL
S,RTC

025 CPU PCH SYS POWER

026 CPU PCH POEWR,GND

027_CPU_PCH_POEWR,GND

028_PCH-SPI ROM,OTH

029 ***

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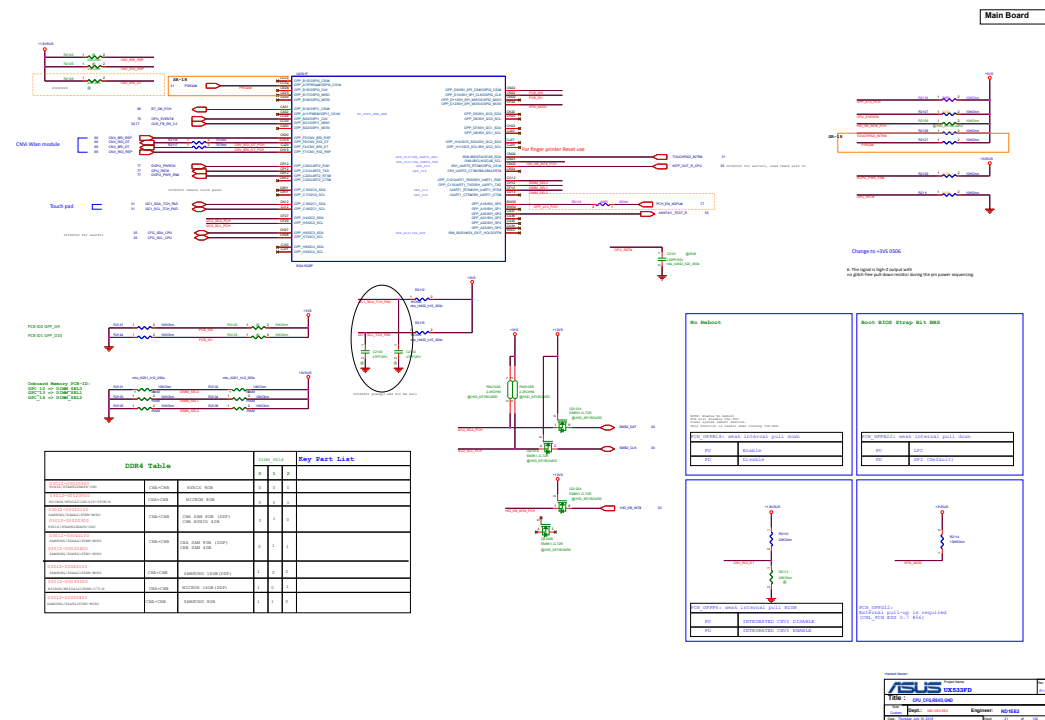
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021_CPU_PCH_CGPIO, LPIO, MI
SC
022_CPU_PCH_AUDIO,SDIO,SD
XC
023_CPU_PCH_PCIE,USB,SATA
024_CPU_PCH_CLOCK SIGNAL
S,RTC
025_CPU_PCH_SYS_POWER
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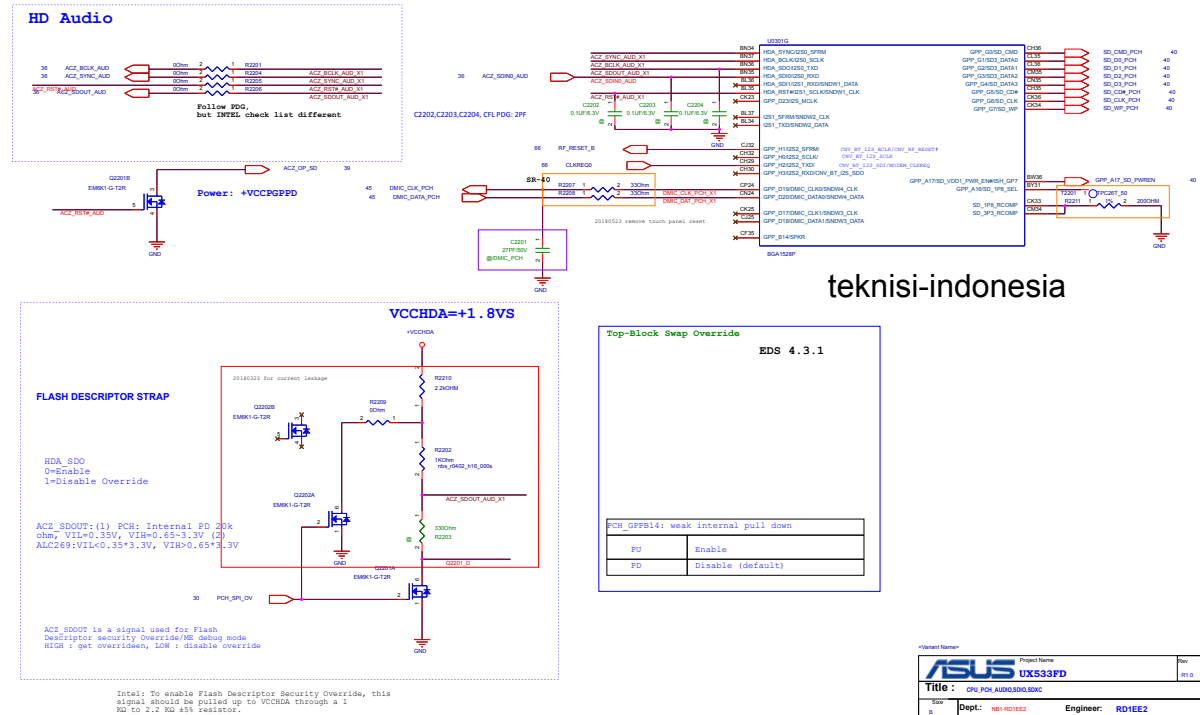
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Project Name		Rev
ASUS UX533FD		01.0
Title : CPU PCH AUDIO,SDIO,SD		
Size	Dept: H&I/EE2	Engineer: RD1EE2
Date: Thursday, Sep 10, 2015	Sheet	22 of 100

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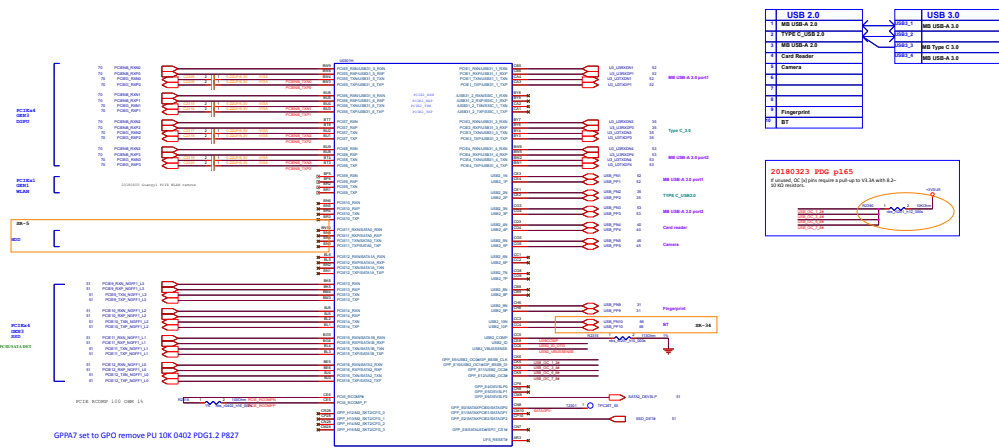
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PCIE 1		Configured to USB3.1	
PCIE 2		Configured to USB3.1	
PCIE 3		Configured to USB3.1	
PCIE 4		Configured to USB3.1	
PCIE 5	X4	GPU	
PCIE 6			
PCIE 7			
PCIE 8			
PCIE 9	X1	WLAN	
PCIE 10		N/A	
PCIE 11		N/A	
PCIE 12		N/A	
PCIE 13	X4	SSD (Lane reverse)	
PCIE 14			
PCIE 15			
PCIE 16			

When used as DSYGLP, no external pull-up or pull-down termination required from SATA Host DSYGLP

R1.2 SATA_DEVSLP change to DEVSLP2

SATA PORT2 0323

PG1-2 P.868 Unused SMDGP[2-3] pins can be left as no-connect and need to be default to GPIO functionality, refer to an unused GPIO for [analog/digital mode](#).



Project Name	
 UX533FD	
Title : CPU, PCN, PCIE, USB, SATA	
Dept.:	RD1EE2

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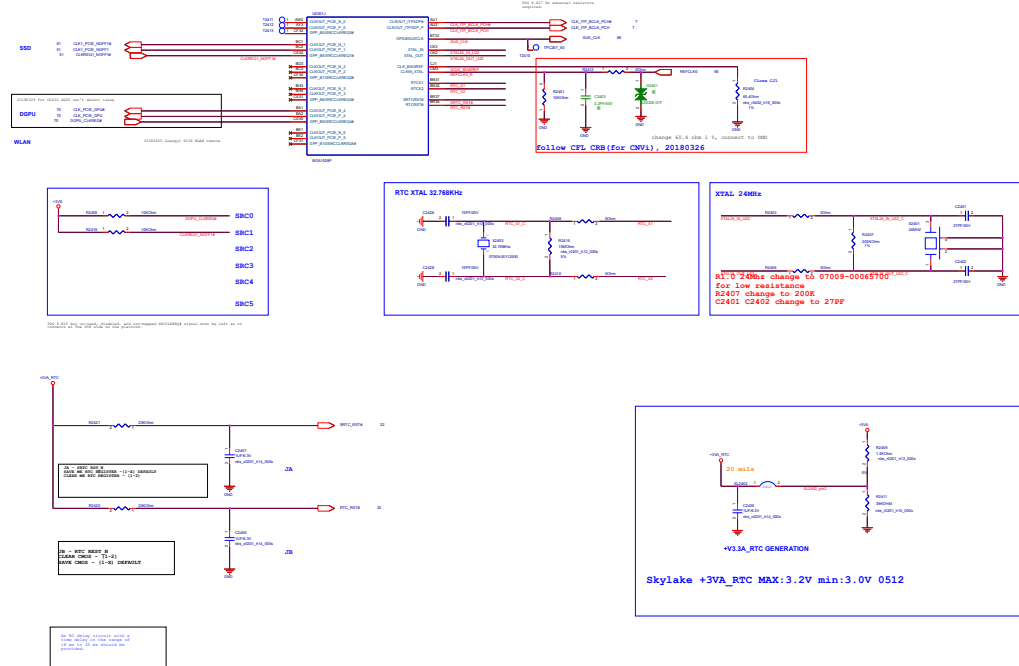
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019 DDR4 CA DQ VOLTAGE

020 CPU PCH CSI2,EMMC,CNV

021_CPU_PCH_CGPIO, LPIO, MI

SC

022_CPU_PCH_AUDIO,SDIO,SD
XC

023 CPU PCH PCIE,USB,SATA

024_CPU_PCH_CLOCK SIGNAL
S,RTC

```
025 CPU PCH SYS POWER
```

026 CPU PCH POEWR,GND

027_CPU_PCH_POEWR,GND

028_PCH-SPI ROM,OTH

029 ***

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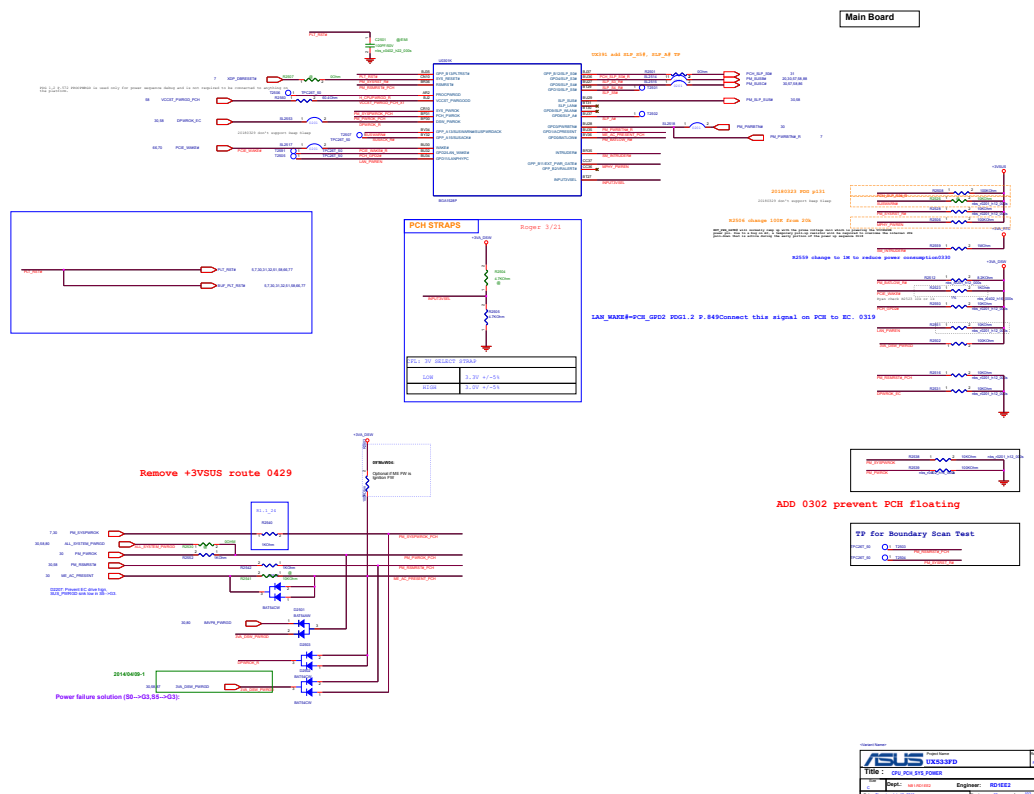
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021_CPU_PCH_CGPIO, LPIO, MI
SC

022_CPU_PCH_AUDIO,SDIO,SD
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023_CPU_PCH_PCIE,USB,SATA
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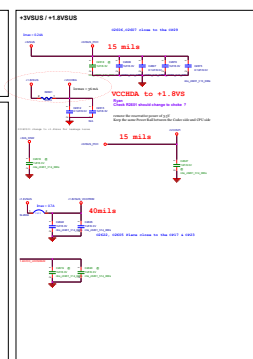
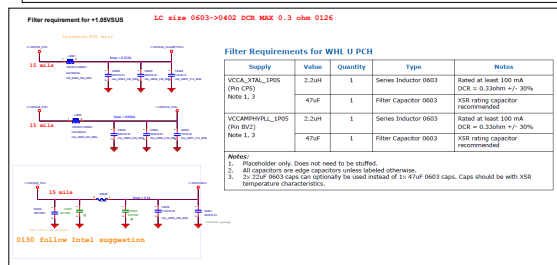
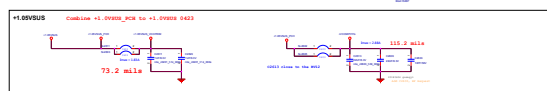
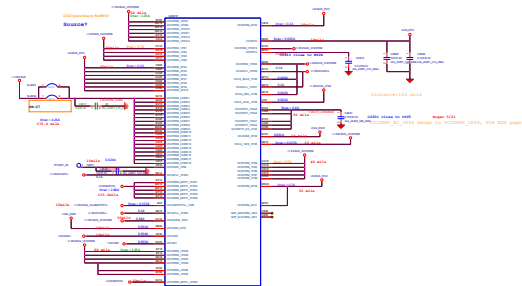
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019_DDR4_CA_DQ_VOLTAGE	
020_CPU_PCH_CSI2,EMMC,CNV	
021_CPU_PCH_CGPIO, LPIO, MI SC	
022_CPU_PCH_AUDIO,SDIO,SD XC	
023_CPU_PCH_PCIE,USB,SATA	
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CP04	VSS_1	VSS_74	BL7
BT0	VSS_2	VSS_74	AE04
BT0	VSS_3	VSS_74	AE04
CP02	VSS_4	VSS_74	AE04
CP02	VSS_5	VSS_77	AE04
BT0	VSS_6	VSS_78	AE04
CP02	VSS_7	VSS_79	AE04
BT0	VSS_8	VSS_80	AE04
BT0	VSS_9	VSS_81	AE04
BT0	VSS_10	VSS_82	AE04
BT0	VSS_11	VSS_83	AE04
BT0	VSS_12	VSS_84	AE04
BT0	VSS_13	VSS_85	AE04
BT0	VSS_14	VSS_86	AE04
BT0	VSS_15	VSS_87	AE04
BT0	VSS_16	VSS_88	AE04
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BT0	VSS_19	VSS_91	AE04
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BT0	VSS_26	VSS_98	AE04
BT0	VSS_27	VSS_99	AE04
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BT0	VSS_30	VSS_102	AE04
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BT0	VSS_38	VSS_110	AE04
BT0	VSS_39	VSS_111	AE04
BT0	VSS_40	VSS_112	AE04
BT0	VSS_41	VSS_113	AE04
BT0	VSS_42	VSS_114	AE04
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BT0	VSS_71	VSS_143	AE04
BT0	VSS_72	VSS_144	AE04

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BT0	VSS_249	VSS_315	AE04
BT0	VSS_250	VSS_316	AE04
BT0	VSS_251	VSS_317	AE04
BT0	VSS_252	VSS_318	AE04
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BT0	VSS_254	VSS_320	AE04
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BT0	VSS_256	VSS_322	AE04
BT0	VSS_257	VSS_323	AE04
BT0	VSS_258	VSS_324	AE04
BT0	VSS_259	VSS_325	AE04
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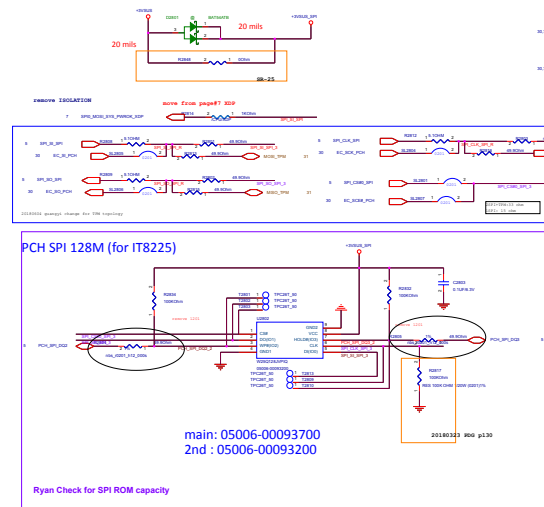
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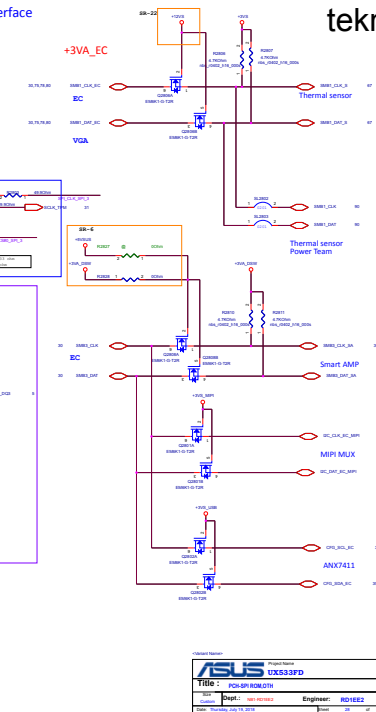
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SPI PCH Power



System Management Interface



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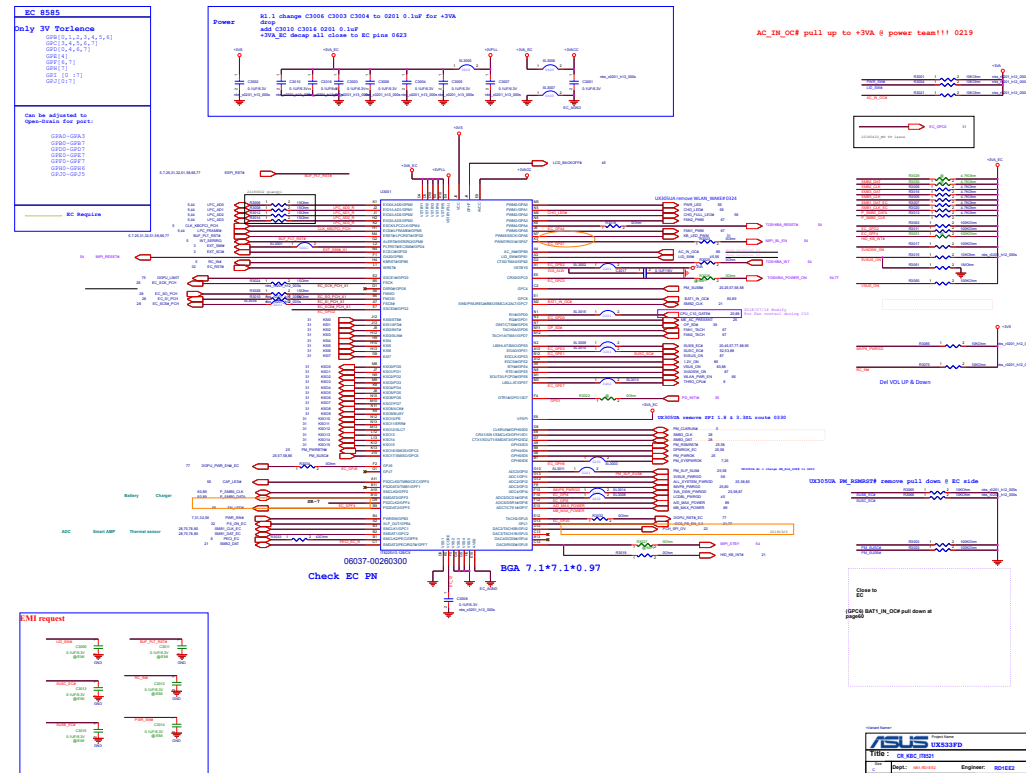
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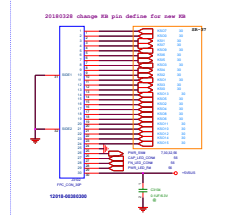
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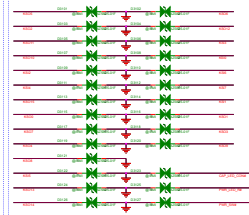
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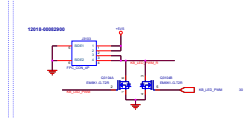
Keyboard



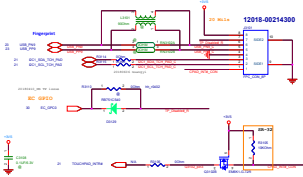
Reserved for EMI



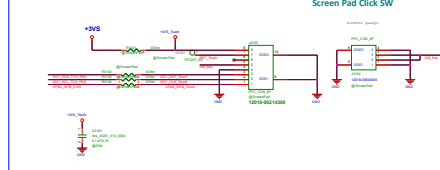
Keyboard BL



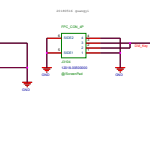
Touch Pad



Screen Pad Touch Con.



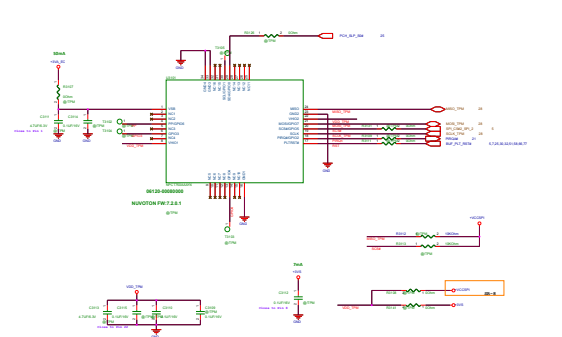
Screen Pad Click SW



EMI solution



TPM



Main Board



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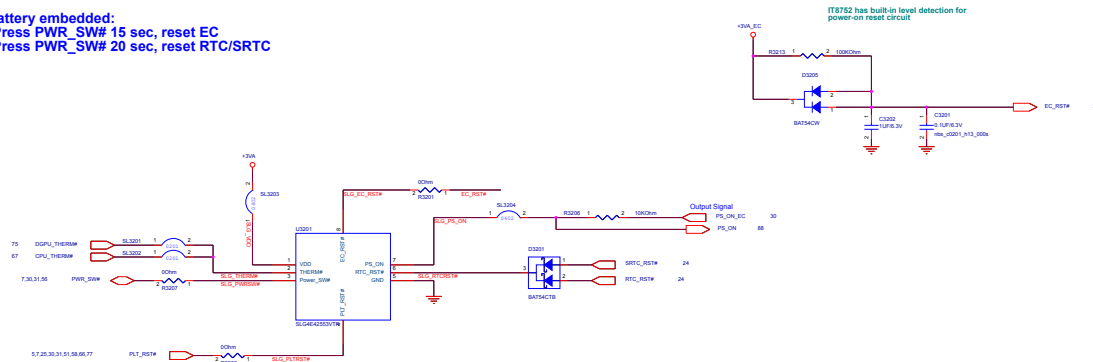
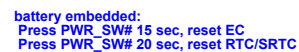
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<div> <div>ASUS</div> <div>Project Name</div> </div> <div>UX533FD</div>		Rev
<div>Title :</div> <div>RST_Rest Circuit</div>		
Size	Dept.: NS1-RD1EE2	Engineer: RD1EE2
D	Date: Thursday, July 15, 2016	Drawn: 32 04 000

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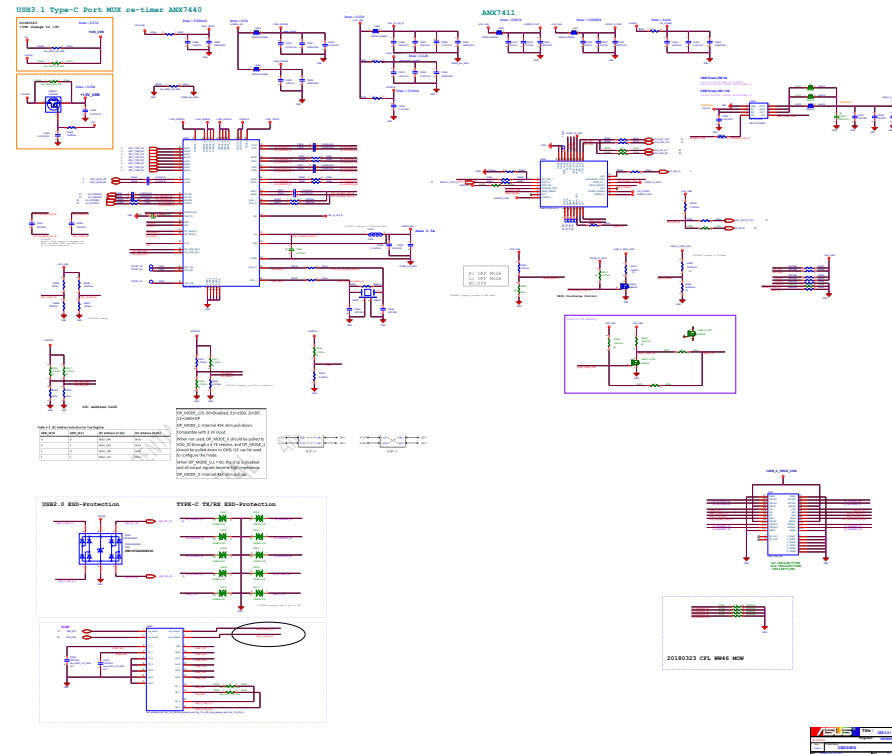
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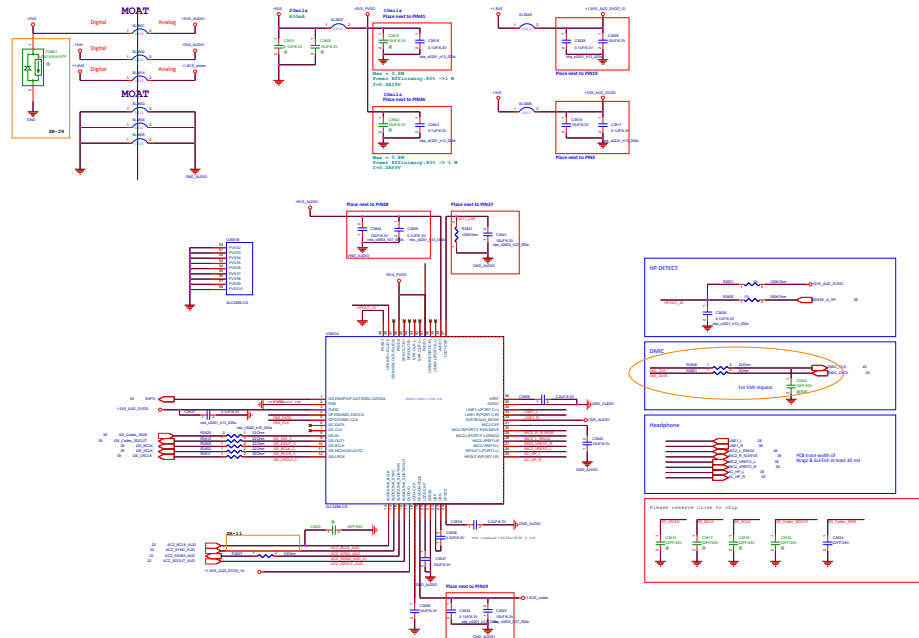
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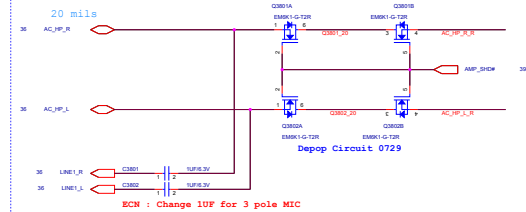
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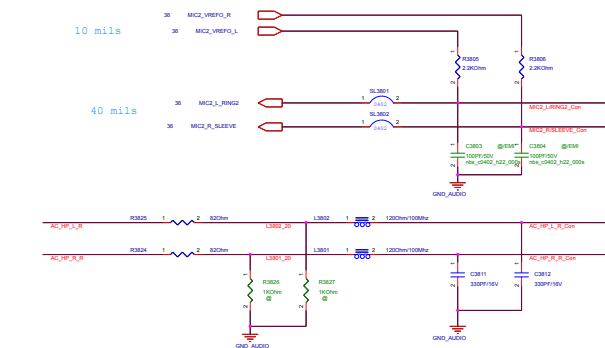
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HP Signal



HP CONN



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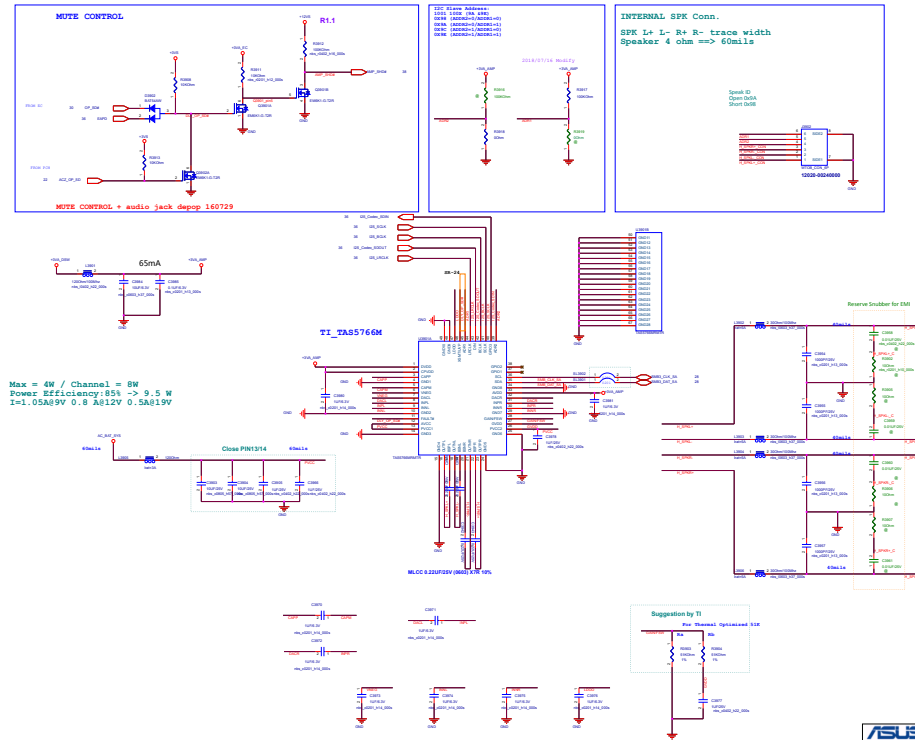
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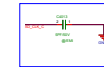
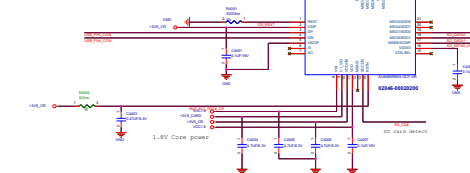
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Card Reader (AD6465RB63-GCF-GR)

Pinout: 1500001
+5VSB AT 500mA max
+5VSB AT 500mA
+5VSB AT 500mA
+5VSB AT 500mA
+5VSB AT 500mA
+5VSB AT 500mA
+5VSB AT 500mA
+5VSB AT 500mA

VDDIO (VDDIO) Transceiver MicroB (Interface) power



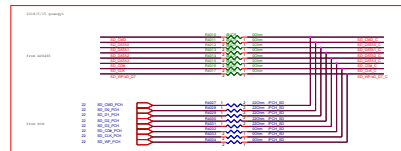
AD write protect

Remove VCC1.8 from VDDIO.
VDDIO is 3.3V I/O pin would output 3.3V
which would affect VCC1.8 when connecting.

Card Reader Connector



Source	Pin	End
1	1	1
2	2	2
3	3	3
4	4	4
5	5	5
6	6	6
7	7	7
8	8	8
9	9	9
10	10	10
11	11	11
12	12	12
13	13	13
14	14	14
15	15	15
16	16	16
17	17	17
18	18	18
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99	99	99
100	100	100



SD Card Power

SD Card Power

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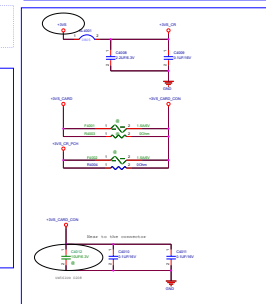
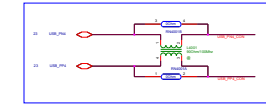
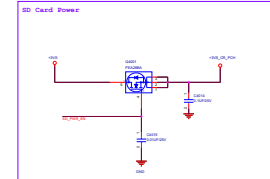
SD Card Power

SD Card Power

SD Card Power

SD Card Power

SD Card Power



ASUS	ASUS
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Part: CB A6465	Part: CB A6465
Rev: 1.0	Rev: 1.0
Doc: CB A6465	Doc: CB A6465
Engineer: R01002	Engineer: R01002

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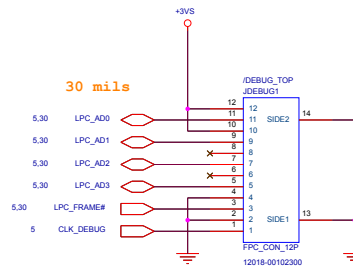
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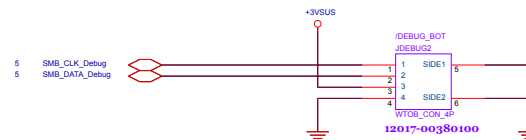
MoveTo

Main Board

LPC Debug Port



DIMM Debug Port

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<Variant Name>		Project Name	Rev
ASUS		UX533FD	R1.0
Title : BUG_Debug			
Size	Dept.:	Engineer: RD1EE2	
A	NB1-RD1EE2		
Date: Thursday, July 19, 2018	Sheet	44	of 102

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025_CPU_PCH_SYS_POWER
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027_CPU_PCH_POEWR,GND
028_PCH-SPI ROM,OTH
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030_KBC_IT8225
031_EC_KB_TP_TPM
032_RESET Circuit
033_****
034_
035_TYPE-C
036_AUD-ALC3288-CG
037_
038_AUD_Headphone
039_AUD_SMA_TSA5766M
040_Card_Reader_AU6465
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042_
043_****
044_BUG_Debug
045_CRT_LCD Panel_CMOS_DMI
C/LID

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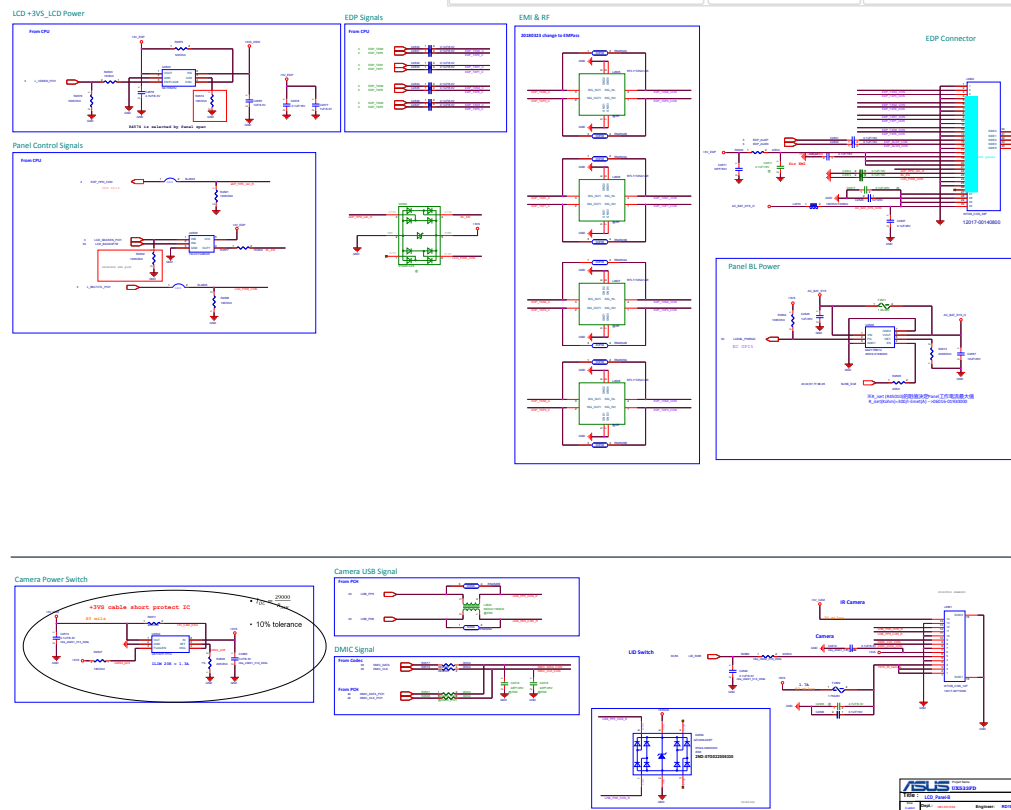
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045_CRT_LCD Panel_CMOS_DMI
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049 HDMI Level Shift MIPI

051 NGFF SSD

053 USB3.1

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057 DSG Discharge

058 PRO Protect

059 ****

060 PW DC JACK / BAT CON

061

062 ME Conn & Skew Hole

063 EMI RF Reserve

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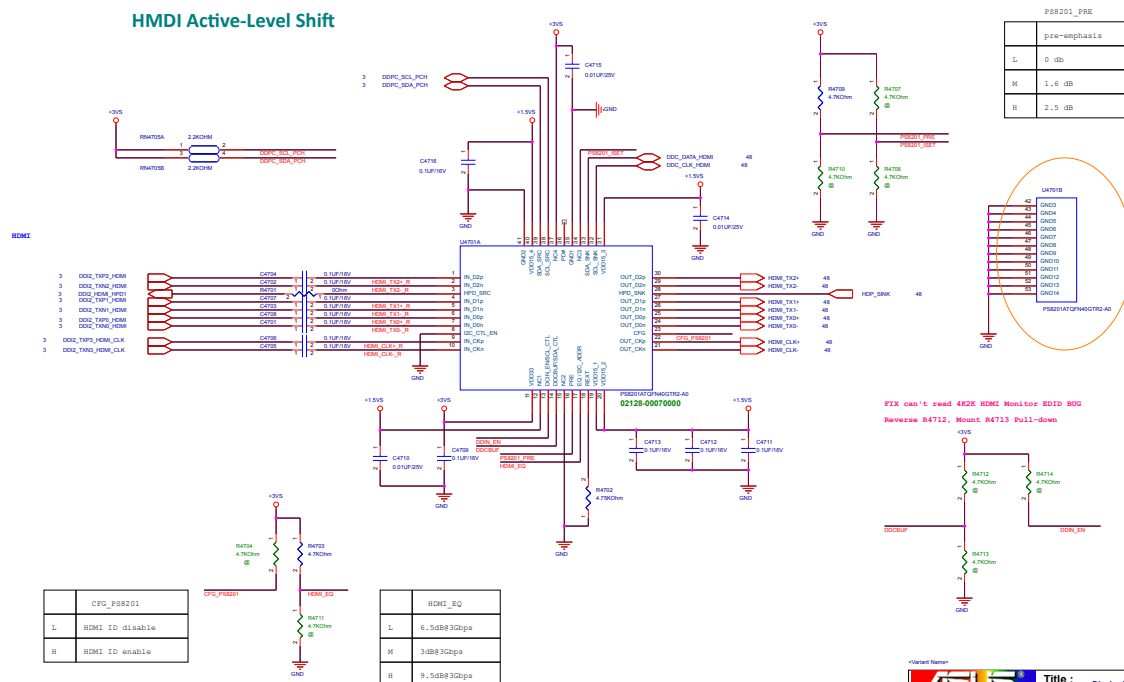
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PSS201 PRE	
	pre-emphasis
L	0 dB
M	1.6 dB
H	2.5 dB

	CFG_PSS201
L	HDMI ID disable
H	HDMI ID enable

	HDMI_EQ
L	6.5dB@3Gbps
M	3dB@3Gbps
H	9.5dB@3Gbps

		Title : Display Port	
RD1-RO1EE2		Engineer: RD1EE2	
Size	Project Name	UX533FD	
ID	Date: Thursday, July 10, 2015	Page: 47	of 50

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051_NGFF_SSD
052_USB3.1
053_USB3.1
054_HDMI to MIPI_TC358779XBG
055_
056_LED_Indicator
057_DSG_Discharge
058_PRO_Protect
059_***
060_PW_DC JACK / BAT CON
061_
062_ME_Conn & Skew Hole
063_EMI_RF Reserve

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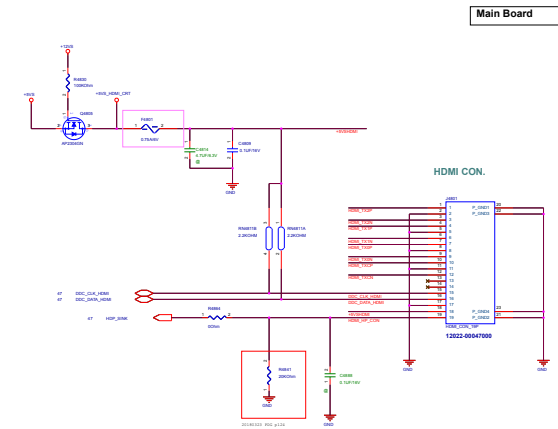
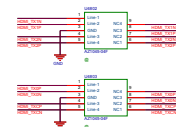
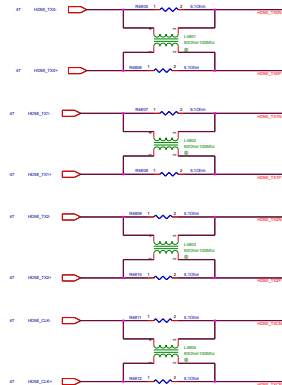
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Close to CONNECTOR
Brewer CON_248211

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045_CRT_LCD Panel_CMOS_DMI
C/LID

047 HDMI Level Shift

049 HDMI Level Shift MIPI

051 NGFF SSD

053 USB3.1

054 HDMI to MIPI TC358779XBG

055

056 LED Indicator

057 DSG Discharge

058 PRO Protect

059 ****

060 PW DC JACK / BAT CON

061

062 ME Conn & Skew Hole

063 EMI RF Reserve

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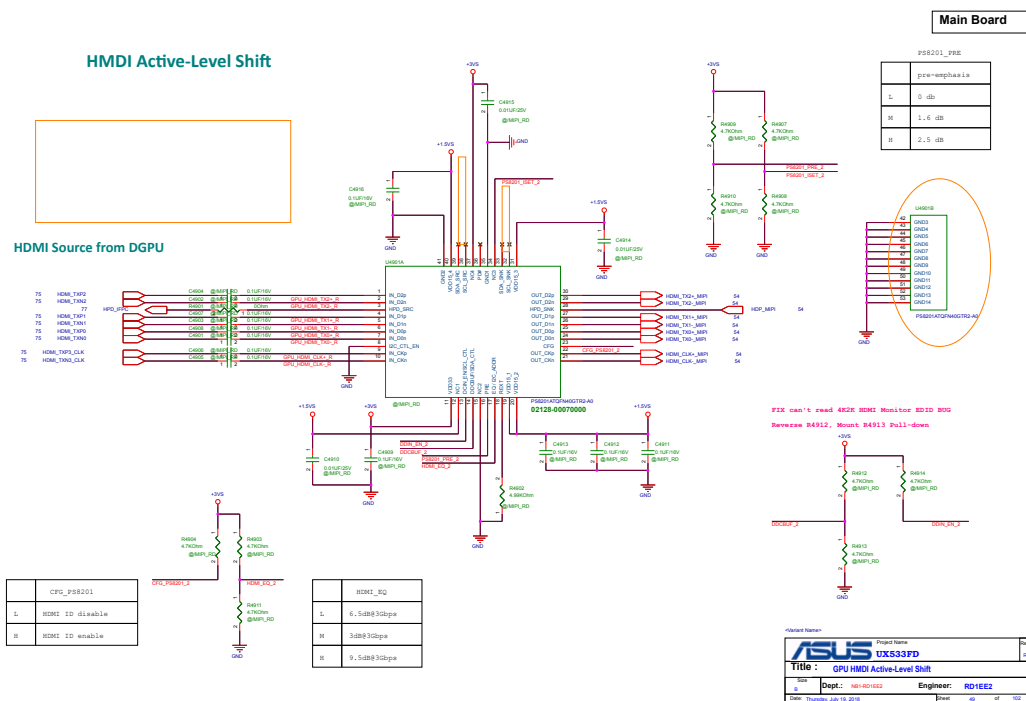
060

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r58201_pre	
	pre-emphasis
L	0 db
M	1.6 db
H	2.5 db

	CFG_PS8201
L	HDMI ID disable
H	HDMI ID enable

	HDMI_EQ
L	6.5dB@3Gbps
M	3dB@3Gbps
H	9.5dB@3Gbps

		Project Name		IS	
UX533FD					
Title : GPU HMDI Active-Level Shift					
Date		Dept.:		Engineer:	
0		NG1-RD1EE2		RD1EE2	
Date: Thursday, July 10, 2008		Email: as		nt 102	

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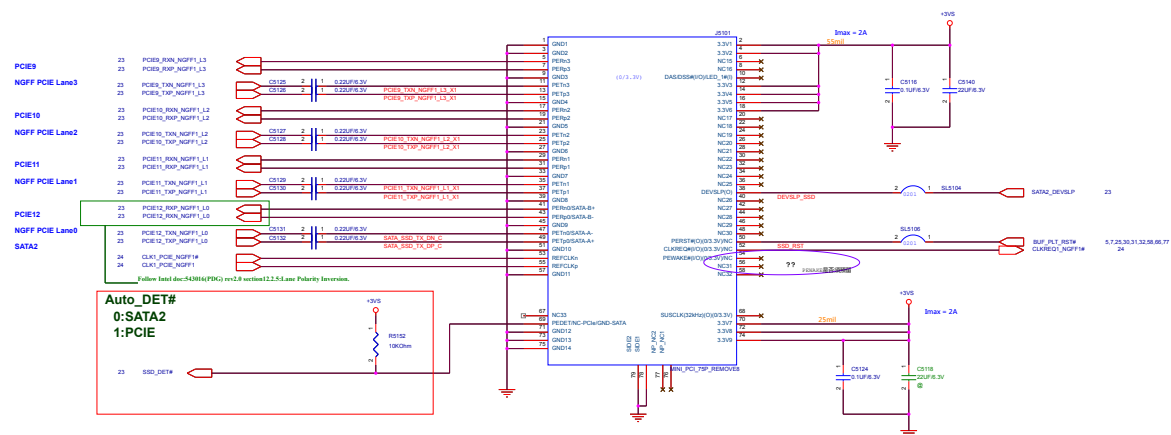
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1st SSD



 Project Name UX533FD		Rev R1.0
Title : MiniCard_SSD		
Size 1	Dept.: NB1-RD1EE2	Engineer: RD1EE2

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063_EMI_RF Reserve

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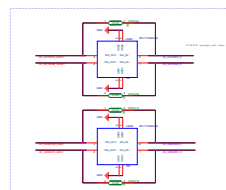
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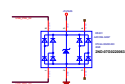
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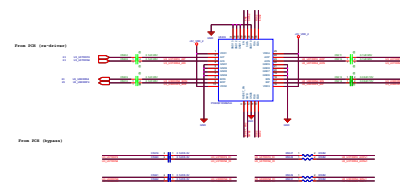
USB3.0_Port 2



USB2.0 ESD-Protection



USB3.0 ESD-Protection

USB3.1 Gen2 Re-Timer IC:
06113-00210000 P138Q1002B1LX

< Pin List Table For Part: USB3.0 (See part sheet) >

Pin	Signal	Function
1	VBUS	Power
2	D-	Differential Data
3	D+	Differential Data
4	GND	Ground
5	NC	Not Connected
6	VBUS	Power
7	D-	Differential Data
8	D+	Differential Data
9	GND	Ground
10	NC	Not Connected

Pin	Signal	Function
1	VBUS	Power
2	D-	Differential Data
3	D+	Differential Data
4	GND	Ground
5	NC	Not Connected
6	VBUS	Power
7	D-	Differential Data
8	D+	Differential Data
9	GND	Ground
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Pin	Signal	Function
1	VBUS	Power
2	D-	Differential Data
3	D+	Differential Data
4	GND	Ground
5	NC	Not Connected
6	VBUS	Power
7	D-	Differential Data
8	D+	Differential Data
9	GND	Ground
10	NC	Not Connected



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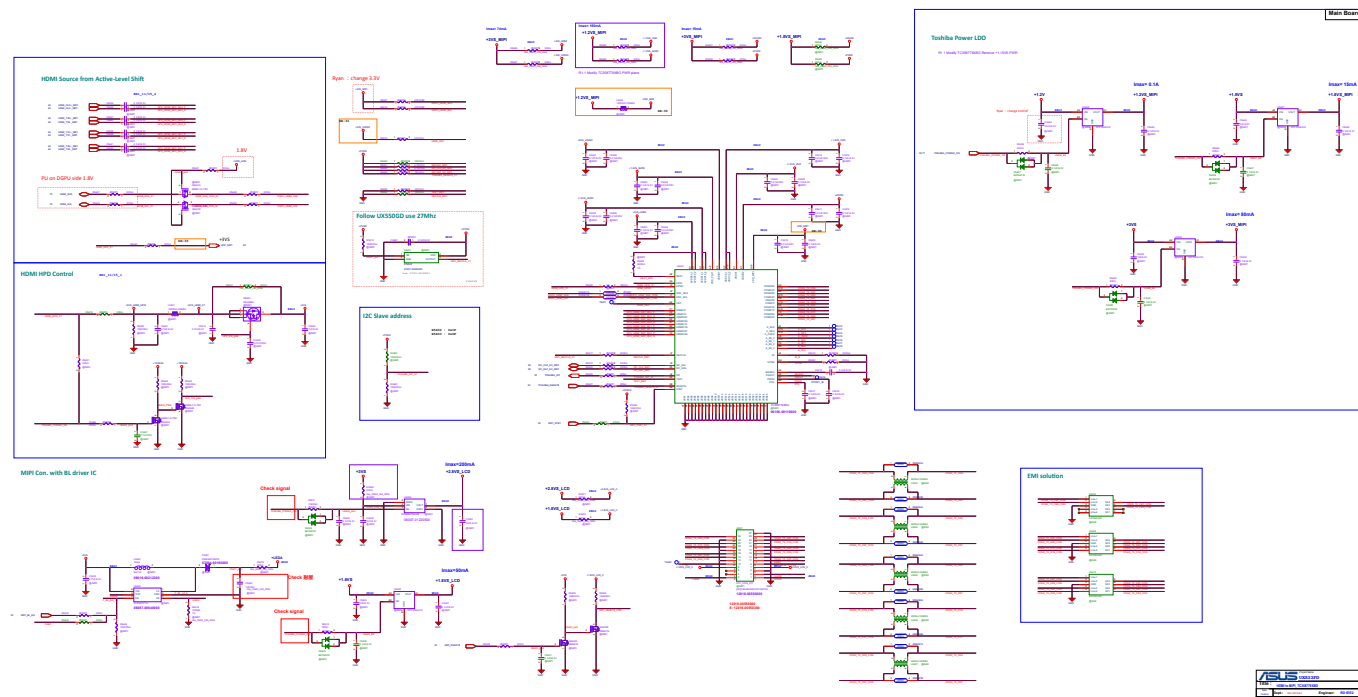
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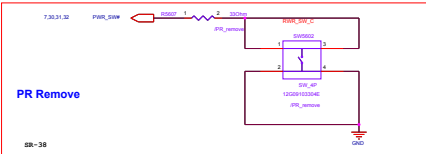
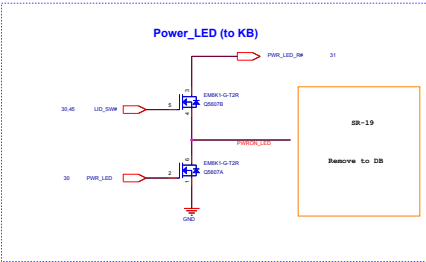
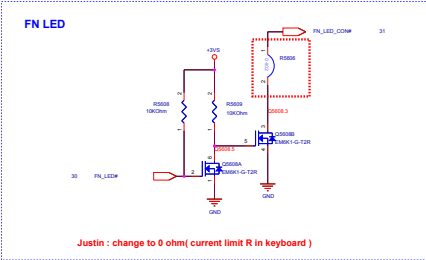
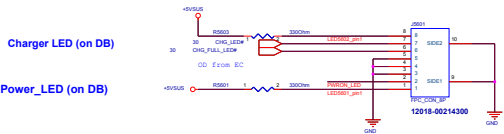
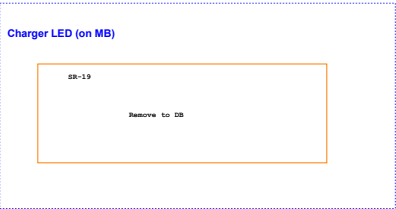
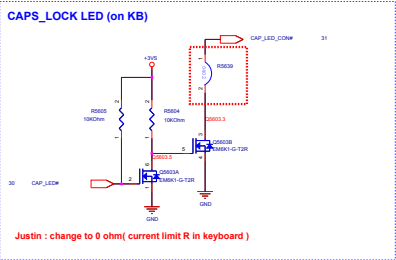
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ASUS	Project Name	Rev
UX533FD	LED Indicator	01.0
Dept: RD1EE2	Engineer: RD1EE2	
Date: November 15, 2018	Print	01 of 102

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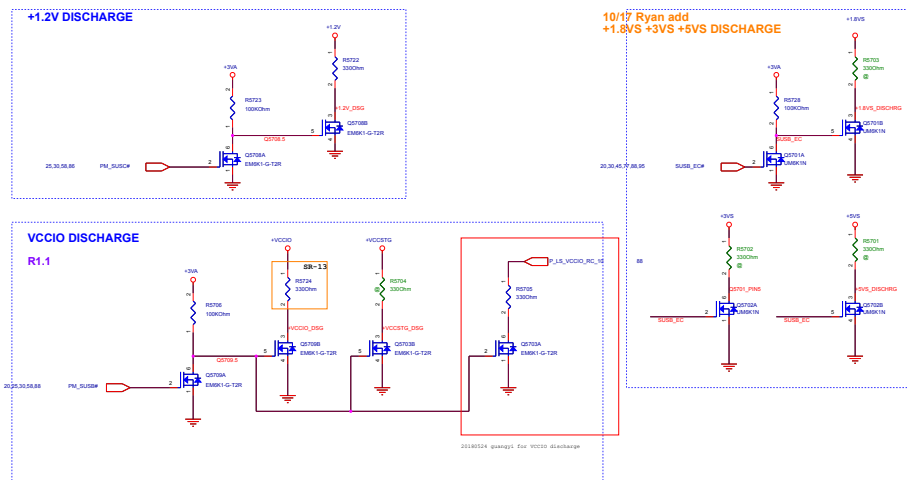
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Justin : Removed no used Discharge circuit
1.8V ,VCCIO,+5VS load switch already build in 180~260 ohm discharge function



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053_USB3.1
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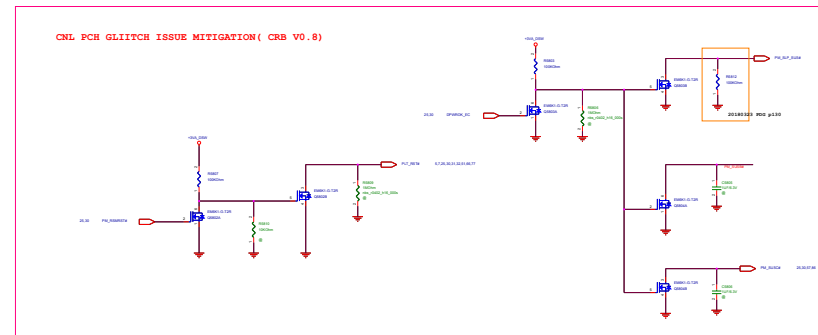
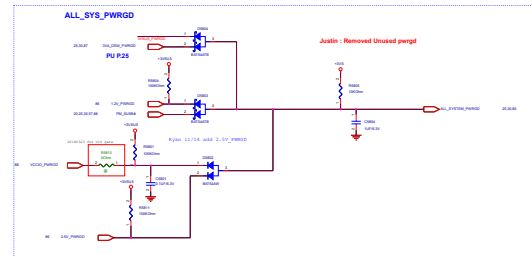
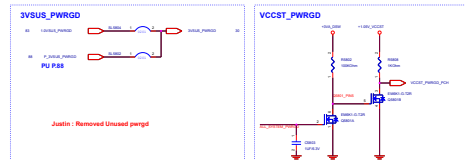
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Main Board

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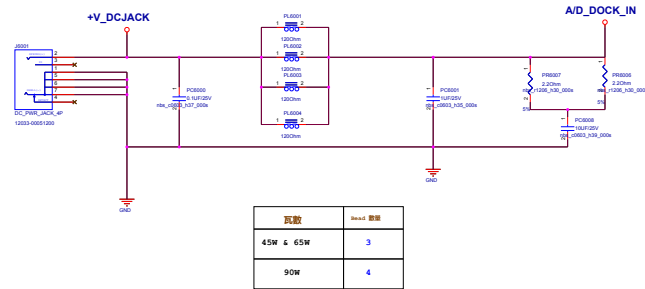
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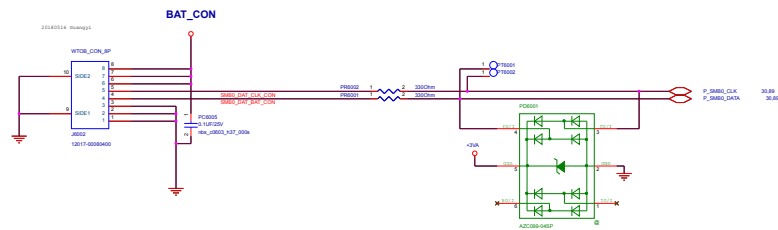
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Battery Connector



ASUS

Project Name	UX533FD	Rev	01.0
Title	DC & BAT Connectors		
Dept.	MSI-HDI/EEZ	Engineer	RD1EE2
Date	Thursday, Aug 19, 2016	Page	65 of 100

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071_GPU_FB-IF_GDDR5(2)

072_FRAME BUFFER-A(3)
073_FRAME BUFFER-B(4)
074_VGA_CRT/LVDS(5)
075_VGA_GPIO/DVI/DP(6)
076_VGA_XTAL/STRAPPING(7)
077_VGA_PWG/GND(8)
078_VRAM Cap/UP1905
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080_PW_WHISKEY LAKE (1)

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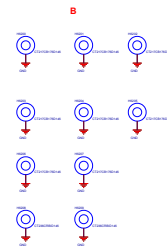
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TOP Side NUT



TOP Side FAN NUT

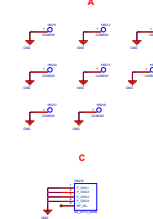
SSD NUT



PAD



Hole



PAD



Tooling_Hole



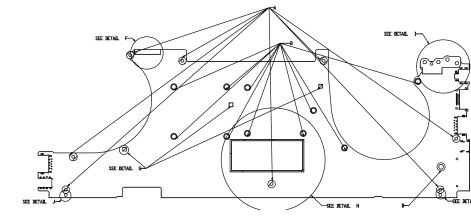
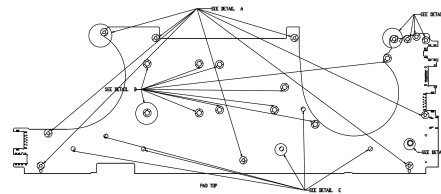
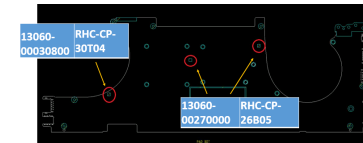
Antenna clip



13060-00030800



13060-00270000



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071_GPU_FB-IF_GDDR5(2)

072_FRAME BUFFER-A(3)
073_FRAME BUFFER-B(4)
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075_VGA_GPIO/DVI/DP(6)
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078_VRAM Cap/UP1905
079_*****
080_PW_WHISKEY LAKE (1)

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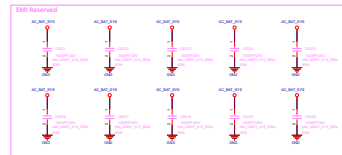
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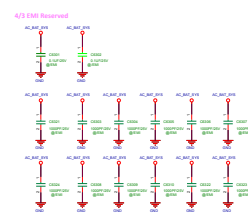
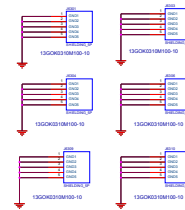
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OR Board BARK CLIP



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077_VGA_PWG/GND(8)

078_VRAM Cap/UP1905

079 *****

080_PW_WHISKEY LAKE (1)

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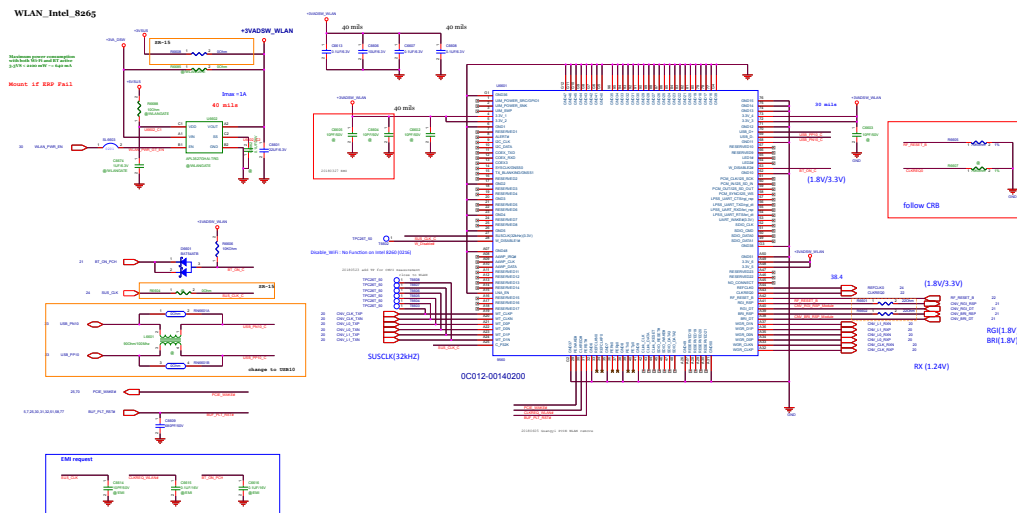
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073_FRAME BUFFER-B(4)

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076_VGA_XTAL/STRAPPING(7)

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079_*****

080_PW_WHISKEY LAKE (1)

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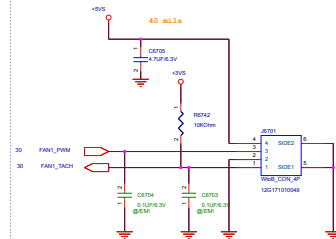
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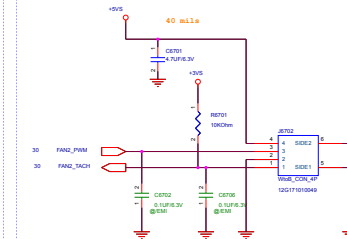
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DC FAN0 Control



DC FAN1 Control



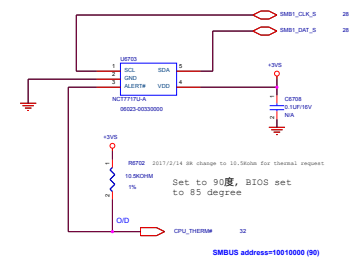
Hall Sensor

LID SW:06045-00050100

reserve to DB

SR-16

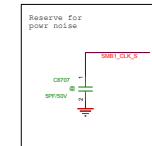
CPU Thermal Sensor



Set to 90 degree, BIOS set to 85 degree

SMBUS address=10010000 (R)

Temp.	Resistor
75	2kOhm
90	7.5kOhm
100	10.5kOhm
105	14kOhm
110	18.7kOhm



ASUS	Project Name	Rev
UX533FD		R1.0
TRIO		
Dept: RD1EE2	Engineer: RD1EE2	
Date: Thursday, 2016-10-20 10:20:18	Drawn: 01	100

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080_PW_WHISKEY LAKE (1)

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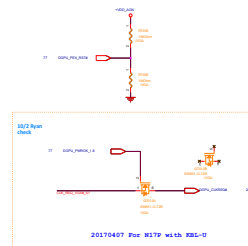
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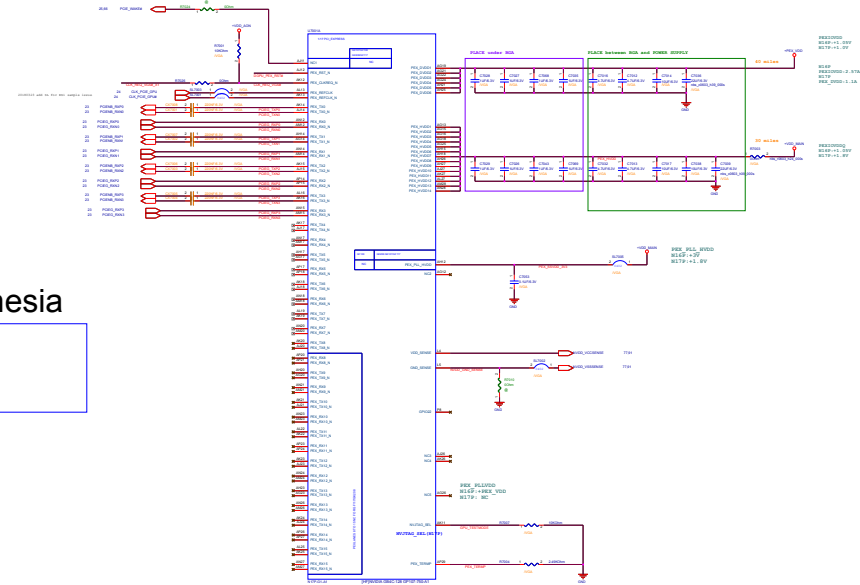
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PCI EXPRESS



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10/2 Ryan combine in Page 77
GPU Power Good
+VDD_ACH/+VDD_MAIN Enable
DGPU PEK_RST



1. R/W 0004-00000000 C: N17P-00-A1 FIRMWARE
WYSSA 0004-00000000 C: N17P-00-A1 FIRMWARE
2. R/W 0004-00000000 C: N17P-01-A1 FIRMWARE
WYSSA 0004-00000000 C: N17P-01-A1 FIRMWARE



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080_PW_WHISKEY LAKE (1)

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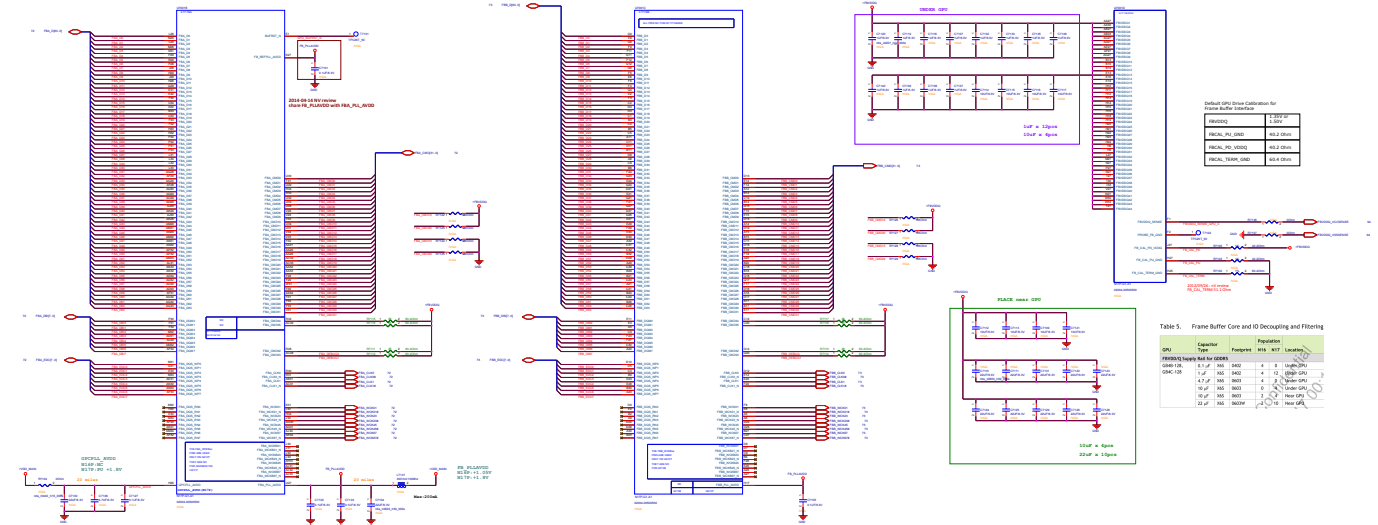
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GPU MEMORY INTERFACE: PARTITION A

GPU MEMORY INTERFACE: PARTITION B



Default GPU Drive Calibration for
Pilot Board for GDDR5

Parameter	Value
GPU_FB-IF	1.000V
GPU_FB-IF_VDD	1.000V
GPU_FB-IF_VDDQ	1.000V
GPU_FB-IF_VDDQ2	1.000V

Table 5. Frame Buffer Core and IO Decoupling and Filtering

GPU	Capacitor	Type	Frequency	Value	Location
GPU FB-IF					
GPU_FB-IF	1.0µF	MLCC	100MHz	1.0µF	GPU_FB-IF
GPU_FB-IF	1.0µF	MLCC	100MHz	1.0µF	GPU_FB-IF
GPU_FB-IF	1.0µF	MLCC	100MHz	1.0µF	GPU_FB-IF
GPU_FB-IF	1.0µF	MLCC	100MHz	1.0µF	GPU_FB-IF
GPU_FB-IF	1.0µF	MLCC	100MHz	1.0µF	GPU_FB-IF

ASUS	
Model	ASUS WHISKEY LAKE
Version	1.0
Author	ASUS
Engineer	ASUS

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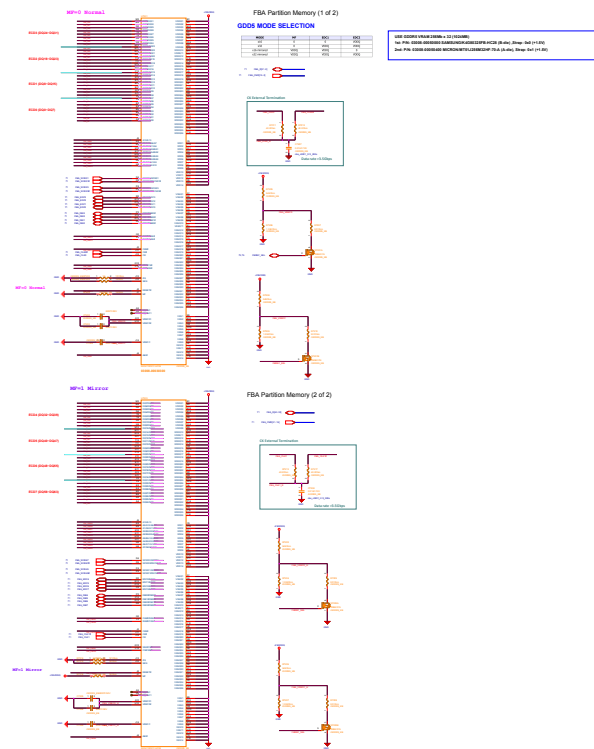
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075_VGA_GPIO/DVI/DP(6)

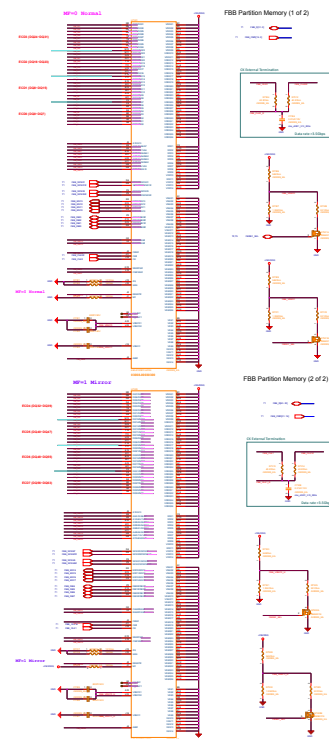
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077_VGA_PWG/GND(8)

078_VRAM Cap/UP1905

079 *****

080_PW_WHISKEY LAKE (1)



USE GOOD VRAM 288Mb or 32 (1024Mb)



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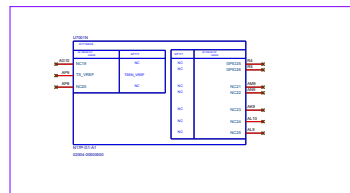
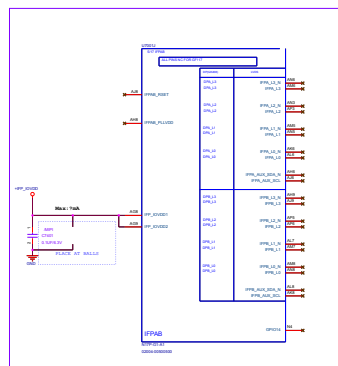
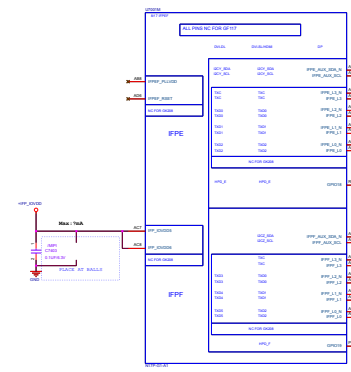
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CRT DAC_A

**LVDS IFPA/B****LVDS IFPE/F**

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073 FRAME BUFFER-B(4)

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075 VGA GPIO/DVI/DP(6)

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077_VGA_PWG/GND(8)

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079 *****

080 PW WHISKEY LAKE (1)

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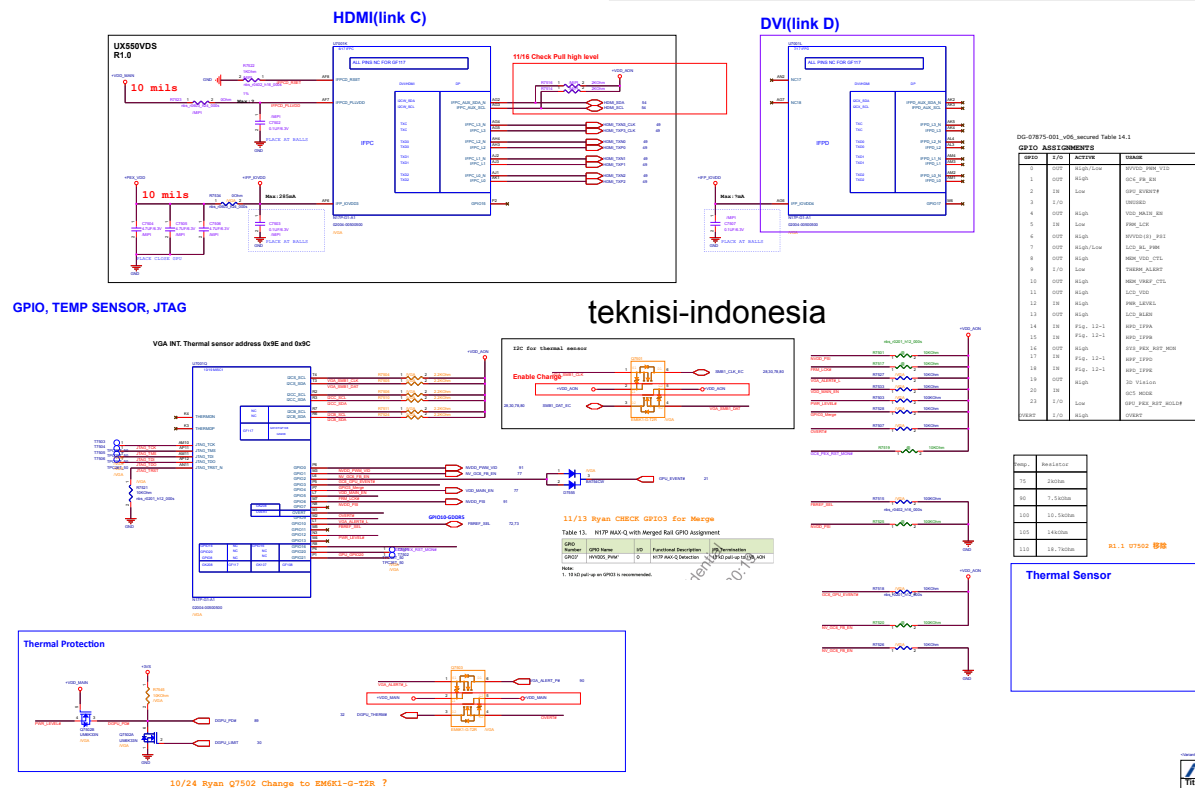
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DESD	1/0	ACTIVE	USAGE
0	0/0	High	MDM_PST_CTL
2	1/0	High	ACT_P3N
2	1/0	Low	ACT_V0V0T7
3	1/0	High	UNREQD
4	0/0	High	MDM_PST_CTL
5	1/0	Low	PMG_LCK
6	0/0	High	PMG_LCK_P1
7	0/0	High	MDM_P3N
8	0/0	High	MDM_PST_CTL
9	1/0	Low	MDM_PST_CTL
10	0/0	High	MDM_PST_CTL
11	0/0	High	MDM_PST_CTL
12	1/0	High	MDM_PST_CTL
13	1/0	High	MDM_PST_CTL
14	0/0	High	MDM_PST_CTL
15	1/0	High	MDM_PST_CTL
16	0/0	High	MDM_PST_CTL
17	1/0	High	MDM_PST_CTL
18	0/0	High	MDM_PST_CTL
19	0/0	High	MDM_PST_CTL
20	1/0	High	MDM_PST_CTL
21	1/0	High	MDM_PST_CTL
22	1/0	High	MDM_PST_CTL
23	1/0	High	MDM_PST_CTL
24	1/0	High	MDM_PST_CTL
25	1/0	High	MDM_PST_CTL
26	1/0	High	MDM_PST_CTL
27	1/0	High	MDM_PST_CTL
28	1/0	High	MDM_PST_CTL
29	1/0	High	MDM_PST_CTL
30	1/0	High	MDM_PST_CTL
31	1/0	High	MDM_PST_CTL

Temp.	Resistor
75	2k00m
90	7.5k00m
100	10.5k00m
105	14k00m
110	18.7k00m

Thermal Sensor

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080_PW_WHISKEY LAKE (1)

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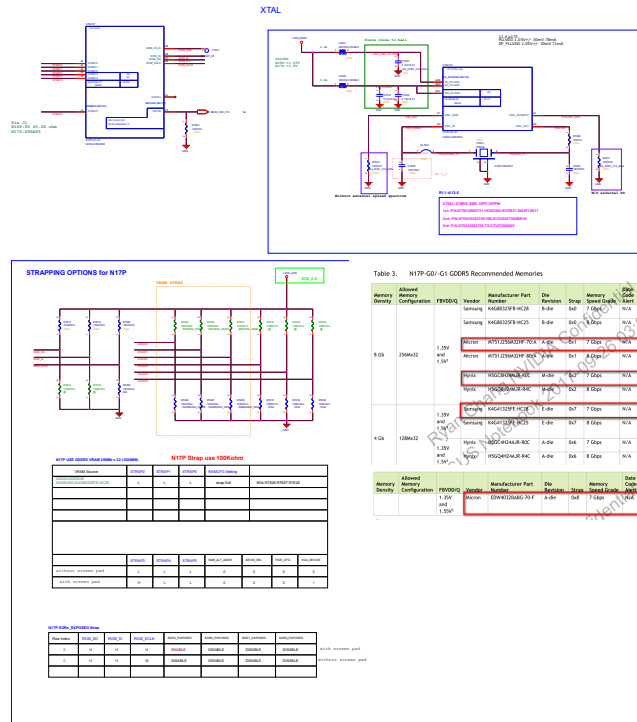


Table 3-1: Signals Link to N17P-G01-G1 GDDR5 Recommended Memories

Signal	Pin	Signal	Pin
STRAP0	1	STRAP1	2
STRAP2	3	STRAP3	4
STRAP4	5	STRAP5	6
STRAP6	7	STRAP7	8
STRAP8	9	STRAP9	10
STRAP10	11	STRAP11	12
STRAP12	13	STRAP13	14
STRAP14	15	STRAP15	16
STRAP16	17	STRAP17	18
STRAP18	19	STRAP19	20
STRAP20	21	STRAP21	22
STRAP22	23	STRAP23	24
STRAP24	25	STRAP25	26
STRAP26	27	STRAP27	28
STRAP28	29	STRAP29	30
STRAP30	31	STRAP31	32
STRAP32	33	STRAP33	34
STRAP34	35	STRAP35	36
STRAP36	37	STRAP37	38
STRAP38	39	STRAP39	40
STRAP40	41	STRAP41	42
STRAP42	43	STRAP43	44
STRAP44	45	STRAP45	46
STRAP46	47	STRAP47	48
STRAP48	49	STRAP49	50
STRAP50	51	STRAP51	52
STRAP52	53	STRAP53	54
STRAP54	55	STRAP55	56
STRAP56	57	STRAP57	58
STRAP58	59	STRAP59	60
STRAP60	61	STRAP61	62
STRAP62	63	STRAP63	64
STRAP64	65	STRAP65	66
STRAP66	67	STRAP67	68
STRAP68	69	STRAP69	70
STRAP70	71	STRAP71	72
STRAP72	73	STRAP73	74
STRAP74	75	STRAP75	76
STRAP76	77	STRAP77	78
STRAP78	79	STRAP79	80
STRAP80	81	STRAP81	82
STRAP82	83	STRAP83	84
STRAP84	85	STRAP85	86
STRAP86	87	STRAP87	88
STRAP88	89	STRAP89	90
STRAP90	91	STRAP91	92
STRAP92	93	STRAP93	94
STRAP94	95	STRAP95	96
STRAP96	97	STRAP97	98
STRAP98	99	STRAP99	100

Table 3. N17P-G01-G1 GDDR5 Recommended Memories

Memory Density	Memory Configuration	Manufacturer Part Number	Die Package	Memory Speed	Memory Type	Die Size	Status
8 Gb	128x64	SanDisk	806	7 Gbps	N/A	Full	Production ready
		SanDisk	806	8 Gbps	N/A	Full	Substitution allowed with vendor
		SanDisk	806	9 Gbps	N/A	Full	Substitution allowed with vendor
		SanDisk	806	10 Gbps	N/A	Full	Substitution allowed with vendor
8 Gb	128x64	SanDisk	806	7 Gbps	N/A	Full	Production ready
		SanDisk	806	8 Gbps	N/A	Full	Substitution allowed with vendor
		SanDisk	806	9 Gbps	N/A	Full	Substitution allowed with vendor
		SanDisk	806	10 Gbps	N/A	Full	Substitution allowed with vendor
8 Gb	128x64	SanDisk	806	7 Gbps	N/A	Full	Production ready
		SanDisk	806	8 Gbps	N/A	Full	Substitution allowed with vendor
		SanDisk	806	9 Gbps	N/A	Full	Substitution allowed with vendor
		SanDisk	806	10 Gbps	N/A	Full	Substitution allowed with vendor

Table 3-2: N17P-G01-G1 GDDR5 Recommended Memories

Strap Pins				Functions Selected by This Strapping			
STRAPS	STRAP4	STRAP5	SAB_ALT_ADDR	DEV0_SEL	PCI_CFG	VGA_SWIO	
L	L	L	0	0	0	0	
L	L	H	0	0	0	0	
L	H	L	0	0	1	0	
L	H	H	0	0	1	1	
H	L	L	0	0	0	0	
H	L	H	0	0	0	1	
H	H	L	0	1	0	0	
H	H	H	0	1	0	1	



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077_VGA_PWG/GND(8)

078_VRAM Cap/UP1905

079_****

080_PW_WHISKEY LAKE (1)

081_PW_WHISKEY LAKE (2)

082_PW_***

083_PW_+1.05VSUS/+1.8VSUS

084_PW_

085_PW_

086_PW_+1.2V/+VTT/+2.5V

087_PW_+3VADSW/+5VSUS

088_PW_LOAD SWITCH

089_PW_CHARGER

090_PW_PROTECTION

091_PW_+NVVDD

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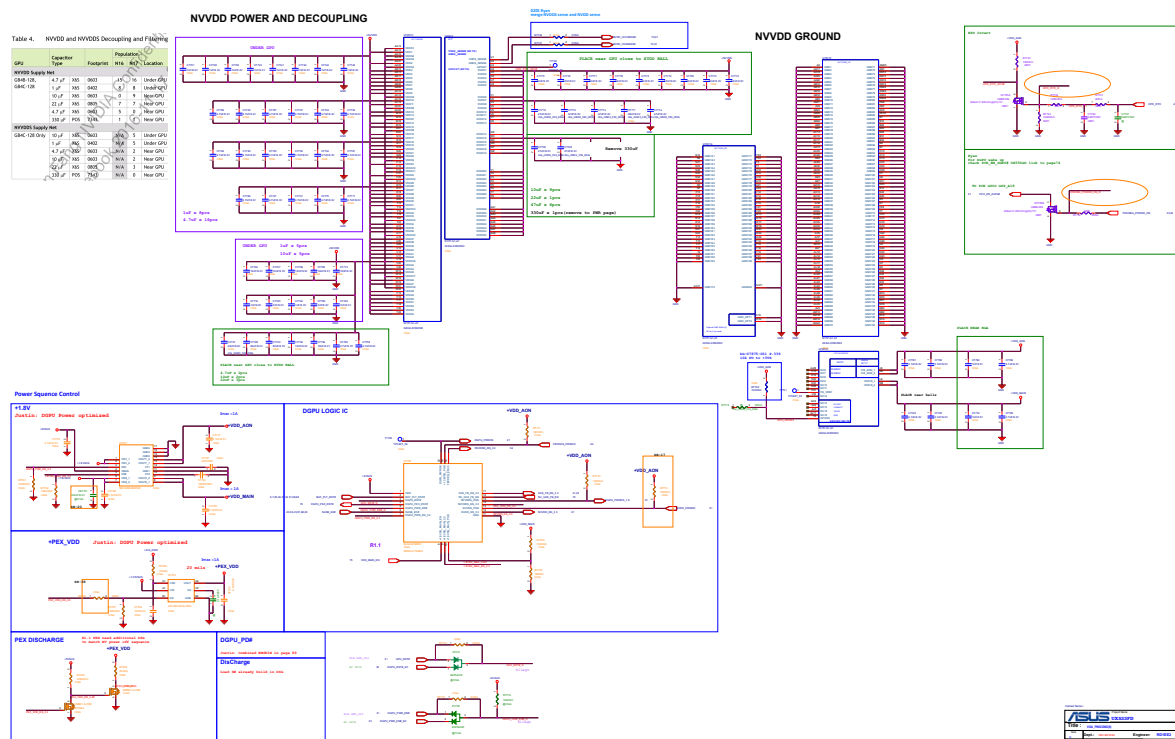
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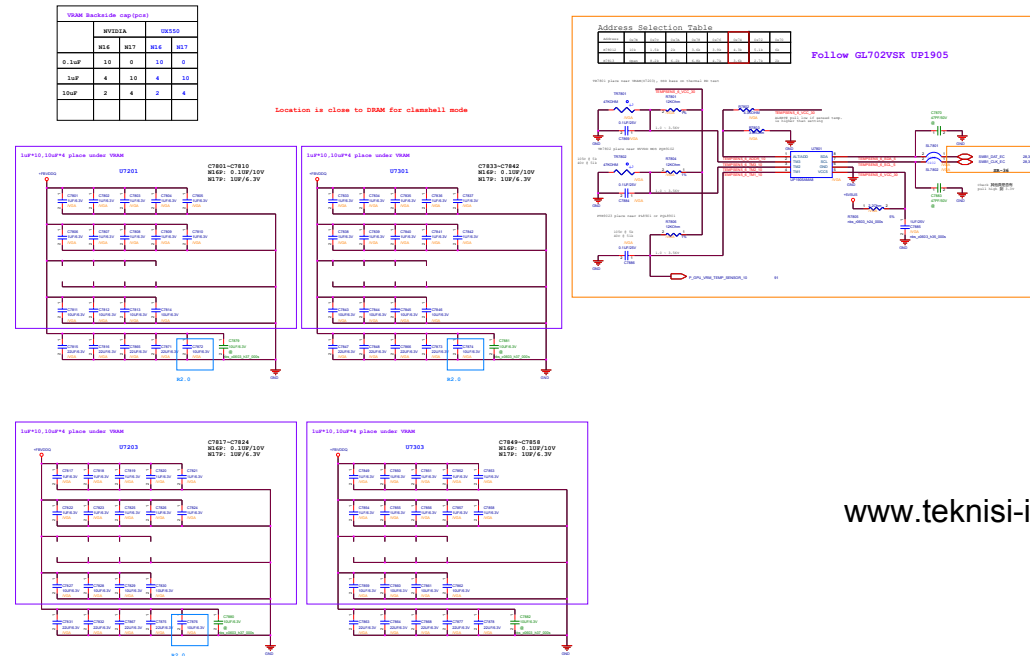
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075_VGA_GPIO/DVI/DP(6)

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088_PW_LOAD SWITCH

089_PW_CHARGER

090_PW_PROTECTION

091_PW_+NVVDD

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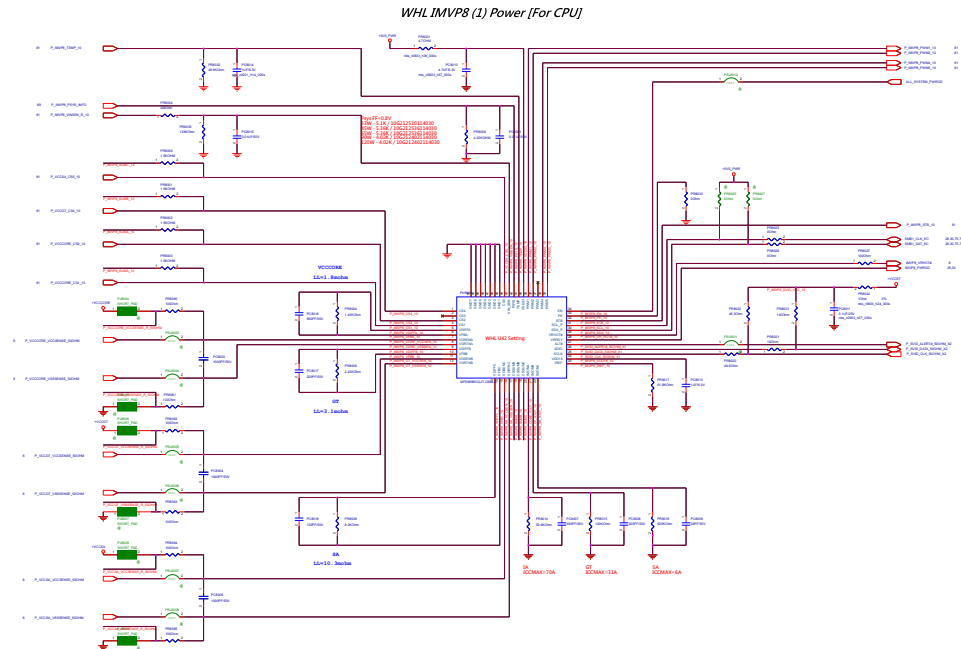
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084_PW_

085_PW_

086_PW_+1.2V/+VTT/+2.5V

087_PW_+3VADSW/+5VSUS

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089_PW_CHARGER

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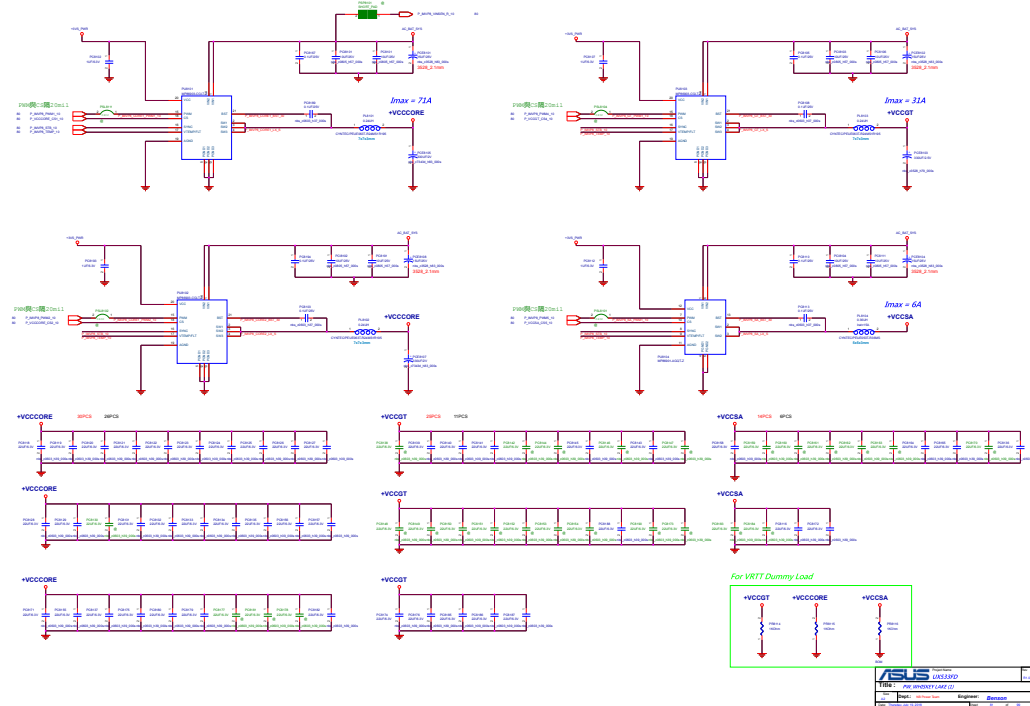
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087_PW_+3VADSW/+5VSUS

088_PW_LOAD SWITCH

089_PW_CHARGER

090_PW_PROTECTION

091_PW_+NVVDD

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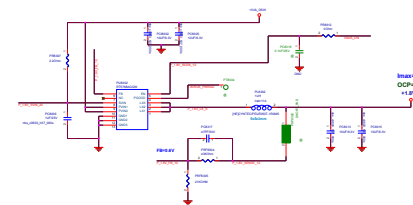
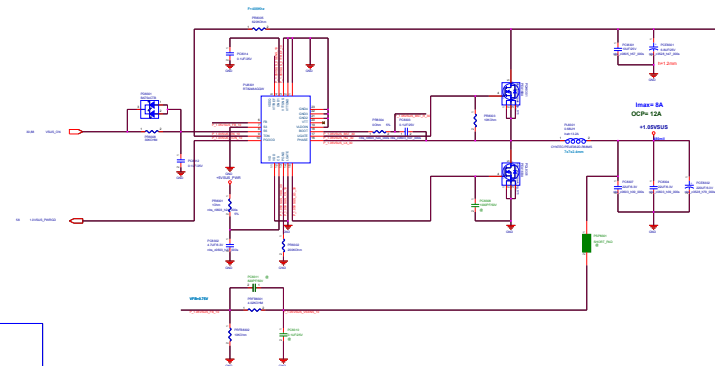
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+1.05VSUS/+1.8VSUS/+1.8VS (For PCH)



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081_PW_WHISKEY LAKE (2)
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084_PW_
085_PW_
086_PW_+1.2V/+VTT/+2.5V
087_PW_+3VADSW/+5VSUS
088_PW_LOAD SWITCH
089_PW_CHARGER
090_PW_PROTECTION
091_PW_+NVVDD

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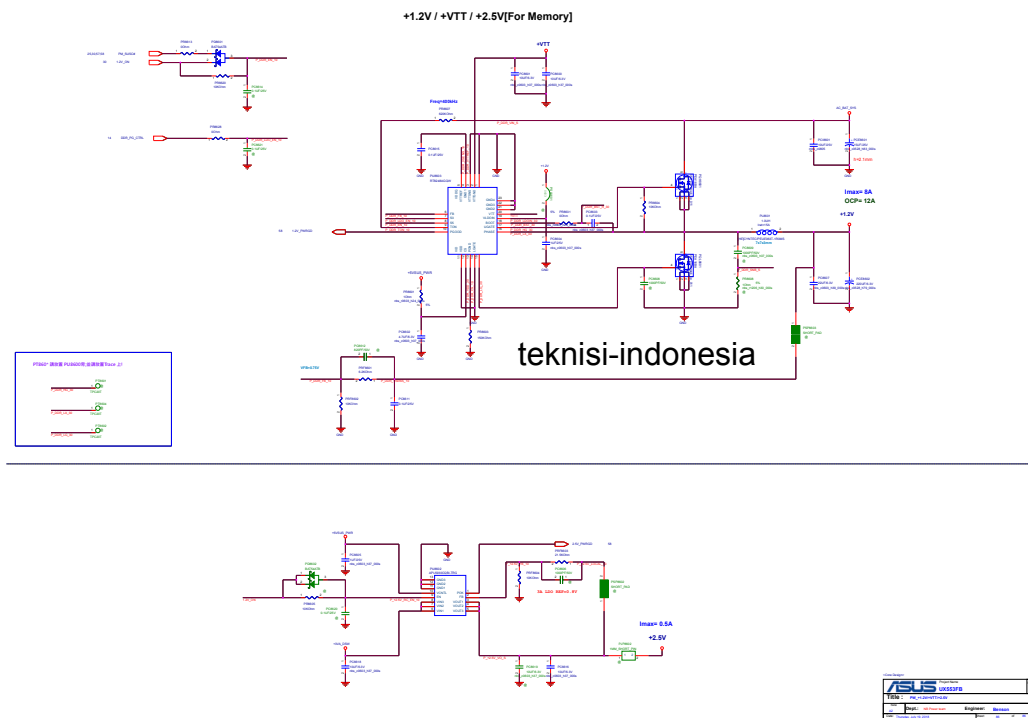
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075_VGA_GPIO/DVI/DP(6)

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077_VGA_PWG/GND(8)

078_VRAM Cap/UP1905

079 *****

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085_PW_

086_PW_+1.2V/+VTT/+2.5V

087 PW +3VADSW/+5VSUS

088_PW_LOAD SWITCH

089_PW_CHARGER

090 PW PROTECTION

091_PW_+NVVDD

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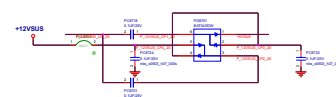
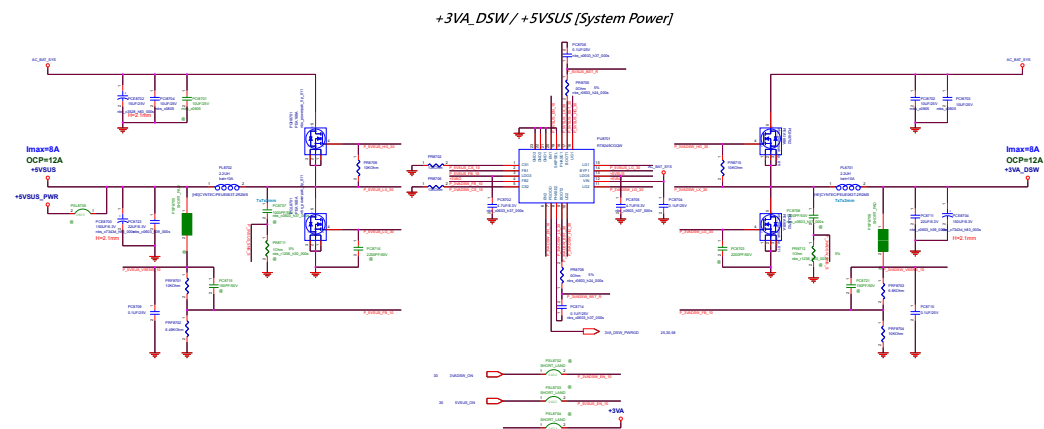
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請 check 零件健康 +12V3AU total 等數對地電壓不得小於100Ohm



	50	55	58	60	65	68	SE with USB Chargers
PIA_ON	1	-	1	-	1	-	1
PIA200M_ON	1	-	1	-	1	-	1
PIA500_ON	1	-	1	-	0	-	0
PIA800_ON	1	-	0	-	1	-	0
1.35V_ON	1	-	1	-	0	-	1
BURST_STOP	1	-	1	-	0	-	0

	B0	C0	S0	003	B4	B0 with USB C (Legacy)
PS_ON	1	1	1	1	0	0
INVRM_ON	1	1	1	1	0	0
INVRM_ON	1	1	1	0	0	0
WBLK_ON	1	1	1	0	0	1
1.3V_ON	1	1	1	0	0	0
BURST_BCP	1	1	1	0	0	0
WBLK_A00	1	1	1	1	1	1



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084_PW_

085_PW_

086_PW_+1.2V/+VTT/+2.5V

087_PW_+3VADSW/+5VSUS

088_PW_LOAD SWITCH

089_PW_CHARGER

090_PW_PROTECTION

091_PW_+NVVDD

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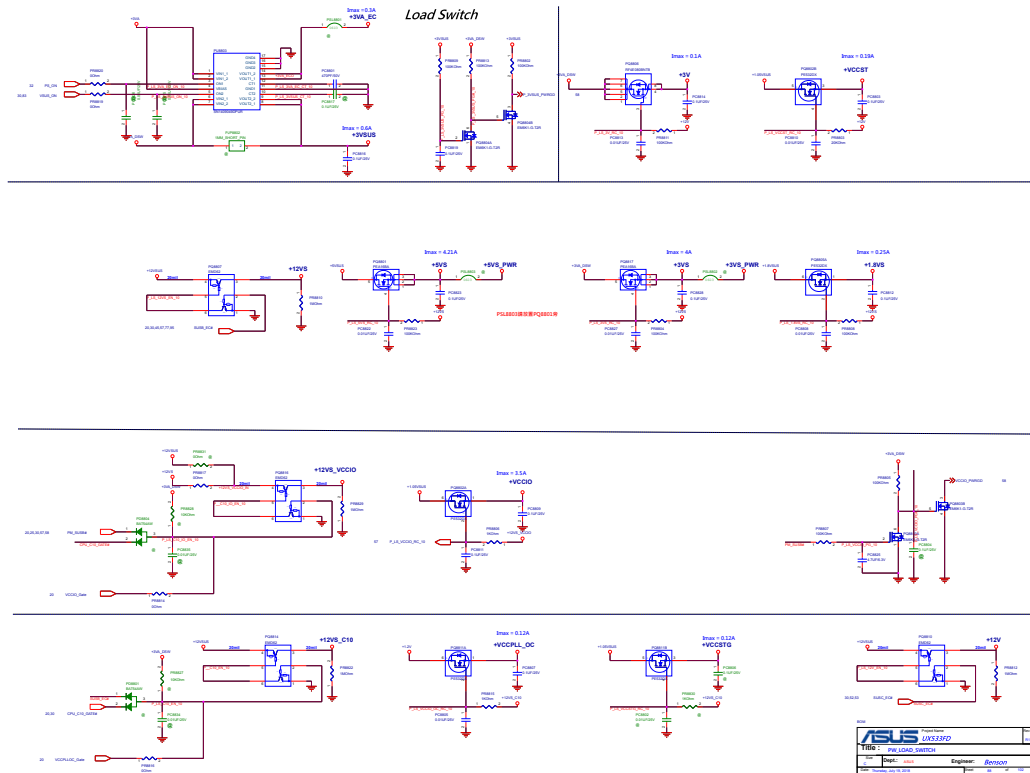
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071_GPU_FB-IF_GDDR5(2)

072_FRAME BUFFER-A(3)

073_FRAME BUFFER-B(4)

074_VGA_CRT/LVDS(5)

075_VGA_GPIO/DVI/DP(6)

076_VGA_XTAL/STRAPPING(7)

077_VGA_PWG/GND(8)

078_VRAM Cap/UP1905

079_*****

080_PW_WHISKEY LAKE (1)

081_PW_WHISKEY LAKE (2)

082_PW_***

083_PW_+1.05VSUS/+1.8VSUS

084_PW_

085_PW_

086_PW_+1.2V/+VTT/+2.5V

087_PW_+3VADSW/+5VSUS

088_PW_LOAD SWITCH

089_PW_CHARGER

090_PW_PROTECTION

091_PW_+NVVDD

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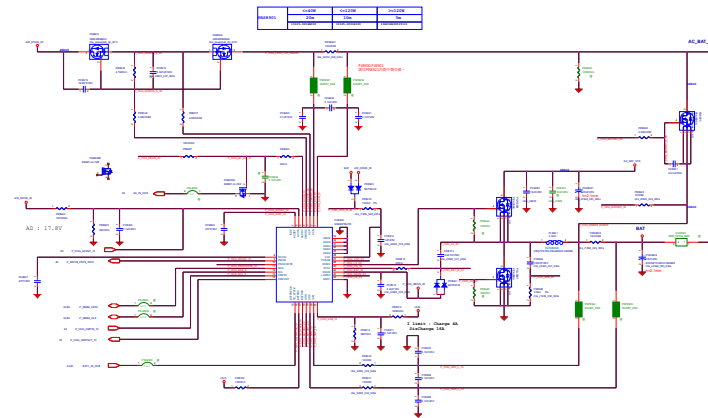
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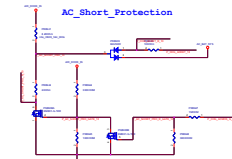
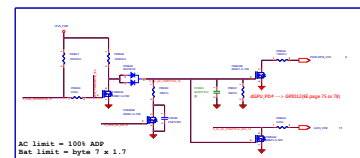
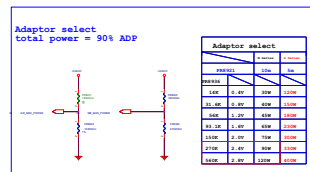
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071_GPU_FB-IF_GDDR5(2)

072_FRAME BUFFER-A(3)

073_FRAME BUFFER-B(4)

074_VGA_CRT/LVDS(5)

075_VGA_GPIO/DVI/DP(6)

076_VGA_XTAL/STRAPPING(7)

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088_PW_LOAD SWITCH

089_PW_CHARGER

090_PW_PROTECTION

091_PW_+NVVDD

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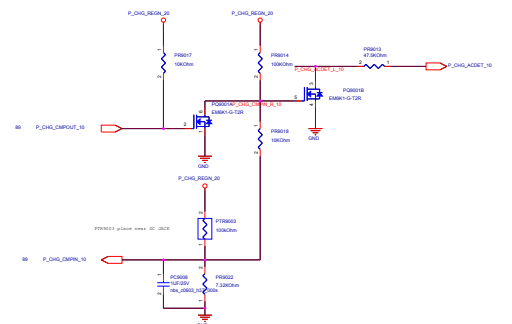
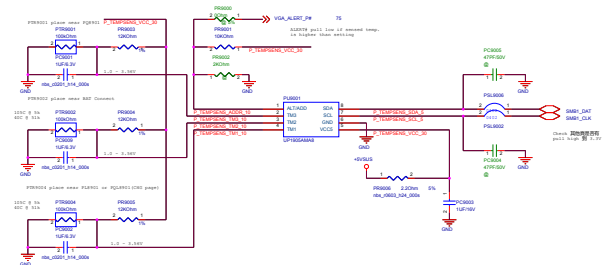
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Pin	Signal	Level	Level	Level	Level	Level	Level
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07008	07009	07010	07011	07012	07013	07014	07015
07016	07017	07018	07019	07020	07021	07022	07023

Register Address

Register	07000	07001	07002	07003	07004	07005	07006	07007
07008	07009	07010	07011	07012	07013	07014	07015	07016
07017	07018	07019	07020	07021	07022	07023	07024	07025
07026	07027	07028	07029	07030	07031	07032	07033	07034



ASUS	Project Name	UX533FD
UX533FD	Project Name	UX533FD
UX533FD	Project Name	UX533FD
UX533FD	Project Name	UX533FD
UX533FD	Project Name	UX533FD

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U/I_GPU_FB-IF_GDDR5(2)
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072_FRAME BUFFER-A(3)

073_FRAME BUFFER-B(4)

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075_VGA_GPIO/DVI/DP(6)

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089_PW_CHARGER

090_PW_PROTECTION

091_PW_+NVVDD

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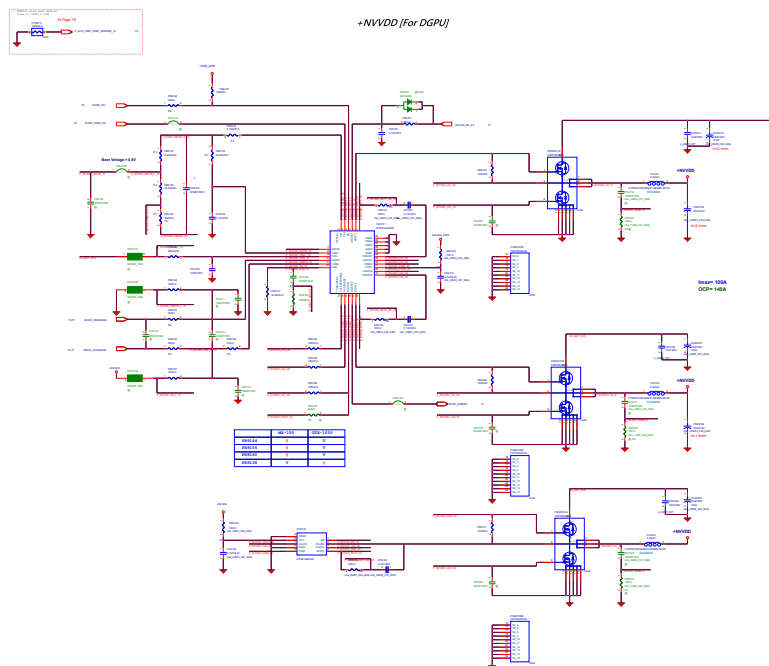
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085_PW_
086_PW_+1.2V/+VTT/+2.5V
087_PW_+3VADSW/+5VSUS
088_PW_LOAD SWITCH
089_PW_CHARGER
090_PW_PROTECTION
091_PW_+NVVDD
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093_PW_
094_PW_+FBVDDQ
095_PW_+1.5VS
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099_PW_FLOW CHART
100_AC Power On Timing

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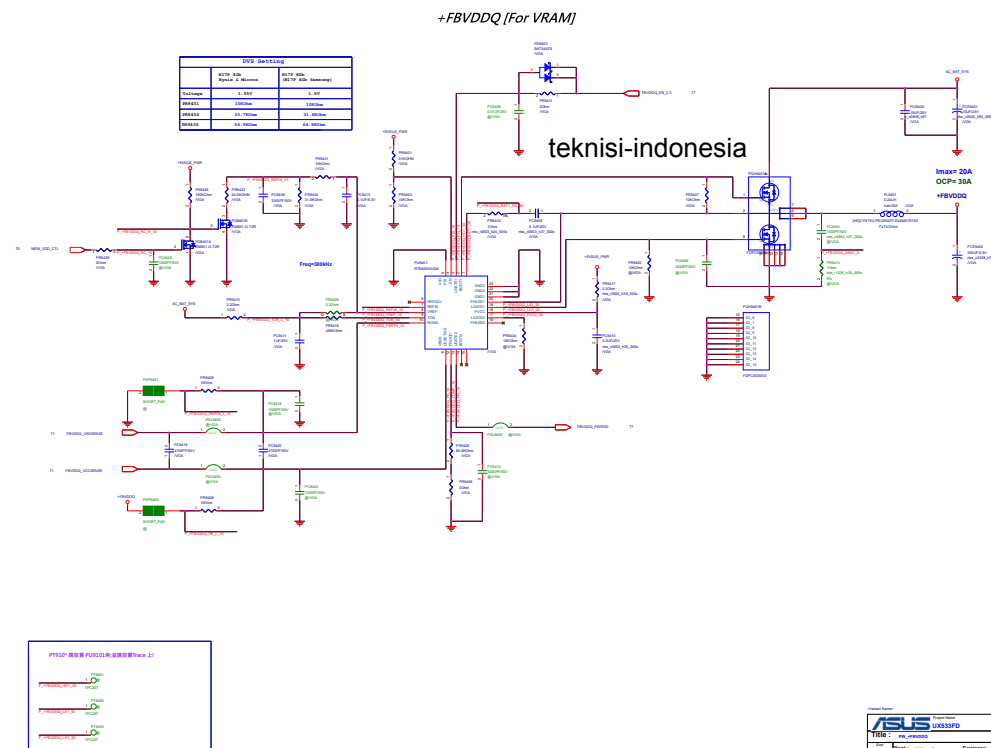
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087_PW_+3VADSW/+5VSUS
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090_PW_PROTECTION
091_PW_+NVVDD
092_PW_***
093_PW_
094_PW_+FBVDDQ
095_PW_+1.5VS
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100_AC Power On Timing

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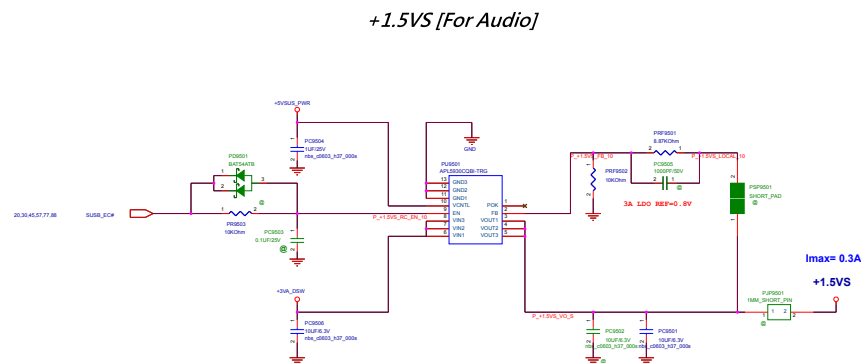
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Richard Norman

		Project Name UX533FD
Title : PW_1.5VS		
Dept.: NSB Power Team	Engineer: Benson	

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080_PW_WHISKEY LAKE (1)
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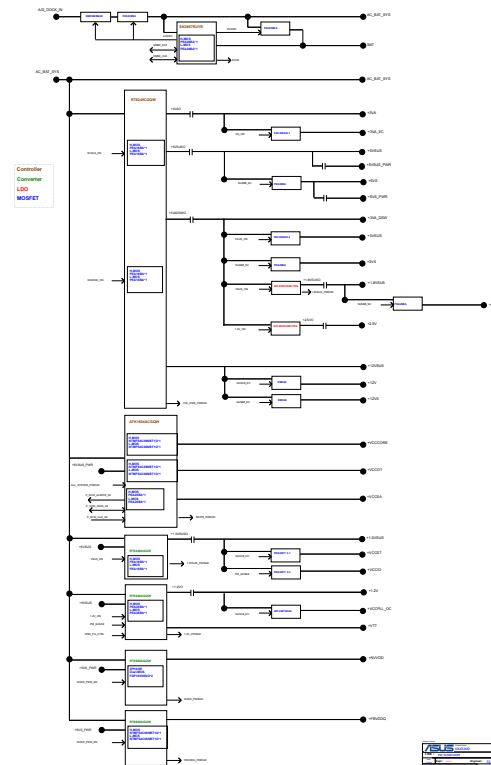
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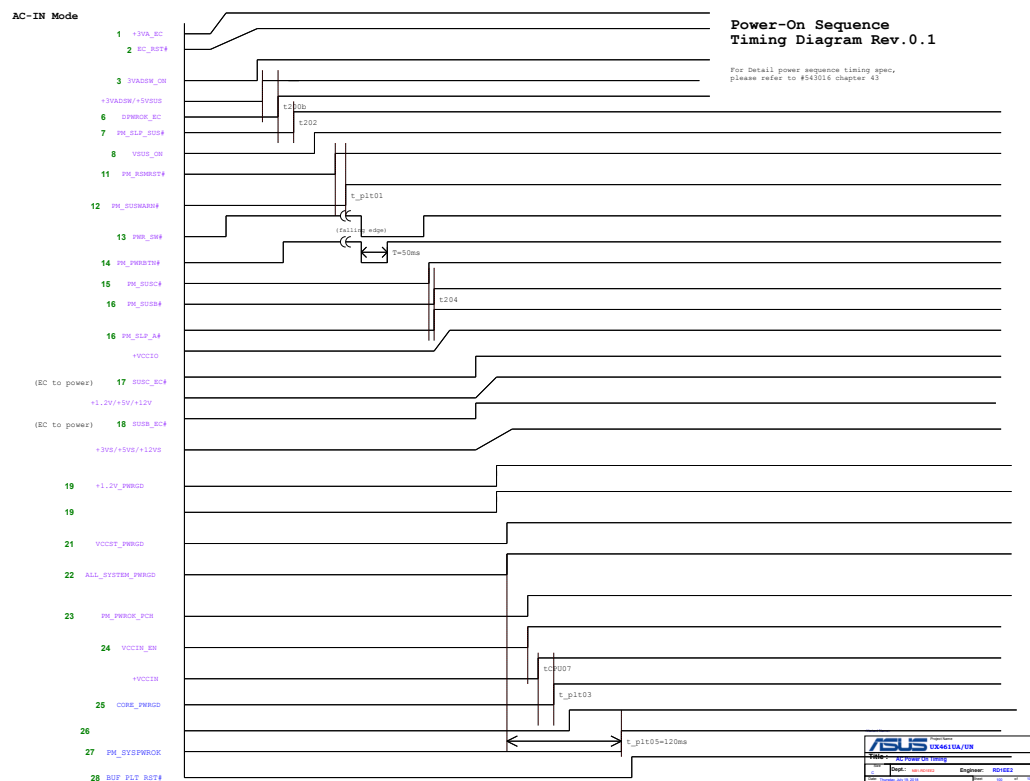
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